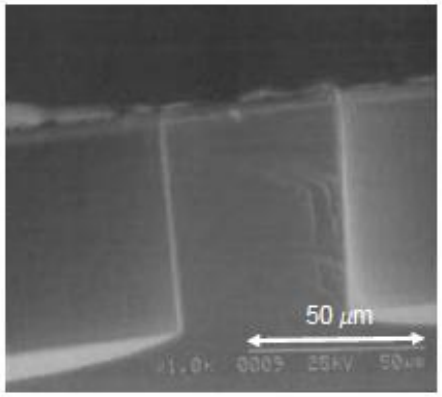
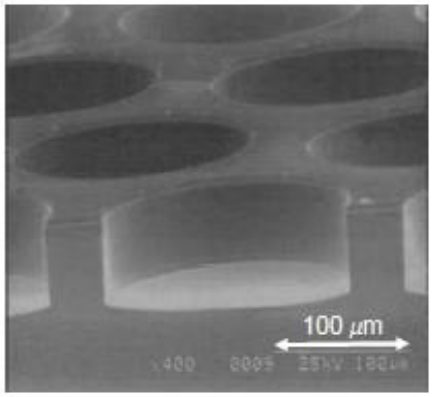
GaAs – Deep Via Etching – Panasonic 1

Process developed by Nathan Jukam.
Resist (Hydrocarbon) passivation required for process.
Always use 6 inch Si carrier wafers whose top surface is coated with SiO2.
Before a series of etches run GaAsClnCoat recipe consisting of 10 minute CF4/O2 clean and 5 minute BCl3/Cl2/Ar coating step. (bias is set to zero)
Attached sample to carrier wafer with diffusion pump oil.
For hole etches use AZ9260 resist as mask.
Spin several layers of AZ4330 resist on two 1-2 square inch SiO2 coated Si wafers.
Mount with diffusion pump oil on opposite sides of samples.
(Note: If you have lots of PR on the sample as a mask (small open area) you might not need the extra samples. With additional resist-coated pieces, SiO2 hard masks may be used)

Standard GaAs Via and air hole etch recipe:

BCl3 40 sccm
Cl2 100 sccm
CF4 0 sccm
Ar 20 sccm
O2 0 sccm
RF Bias 100 Watts
RF ICP 900 Watts
Pressure 7 Pascals





Etch Rate: ~7um/min for 1:2 Aspect ratio and PR passivation.
~10um/min for very open area with no PR passivation.
Selectivity with PR: ~10:1 for via holes
Selectivity with SiO2: ~90:1 for low aspect ratio open areas