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Photolithography of SU8-2005

Objective: To set up photolithography process of SU8-2005.

Experimental:

1)Sample (Si pieces) preparation: a) Soaking in acetone (2') and iso-propanol (2') in ultrasonic bath, then, nitrogen gas dry; b) Soaking in Nano strip tank at 70^{o}C for 10 minutes, then, DI water rinse and nitrogen gas dry; c) Oxygen plasma treatment to make surface hydrophobic (PEII): 300mT/100 W for 30"; d) Dehydration bake at 200^{o}C for 10 minutes (let it cool down on metal surface for 5 minutes).

2) Lithography:
a) Spin-on HMDS. 2500 rpm for 30".
b) Spin-on SU8-2005. Two steps: first one: 500 rpm with 100 rpm/s ramp for 8"; second one: 2500rpm with 300 rpm/s for 30".
c) Soft bake at 95^{o}C for 3 minutes, then, let it cool down on cleanroom paper for 5 minutes.
d) Resist bead removal using acetone and Q-tip.
e) Resist expose using MA-6, mask with 12μm-ridge-lines, and a UV Filter (HOYA UV-34, 200-750 nm) for sample#13 only: cutting the transmission off by 50% at 350 nm.
f) Post expose bake at 95^{o}C for 3 minutes, then, let it cool down on cleanroom paper for 5 minutes.
g) Development in SU8 developer: in the first developer bath for 60", then, in the second fresh developer bath for 15", then, rinse the sample with isopropanol and soak in isopropanol for 20", then, nitrogen gas dry.
h) Post development bake at 200^{o}C for 10 minutes (to improve the resist adhesion on Si substrate).
i) O_2 plasma etch on some samples using RIE#5: 5mT, 150W, O_2 flow-rate=20 sccm.

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Result and Discussion:

Table 1.

Sample#	Soft-bake Temperature (^{o}C)		Expose (CH1=18.4mW; CH2=17.2mW)			Post-exposure-bake Temperature (^{o}C) and (time)		Development Time (s)		Post-development-bake Temperature (^{o}C)	SU8-2005 adhsion to substrate
	Pre-bake	Bake	Expose Time (s)	Contact Mode	UV Filter	Pre-bake	Bake	Bath#1	Fresh Beth#2		
1	65 (2')	95 (5')	6	Hard	none	65 (2')	95 (5')	45	15	none	not good: peeled off
2	65 (2')	95 (5')	9	Hard	none	65 (2')	95 (5')	45	15	none	not good: peeled off
3		95 (2')	12	Hard	none		95 (3')	60	20	none	not good: peeled off
4	65 (2')	95 (5')	6	Hard	none	65 (2')	95 (5')	45	15	200 (10')	good
5	65 (2')	95 (5')	9	Hard	none	65 (2')	95 (5')	45	15	200 (10')	good
6		95 (2')	4	Hard	none		95 (3')	45	15	200 (10')	good
7		95 (2')	5	Hard	none		95 (3')	45	15	200 (10')	good
8		95 (2')	6	Hard	none		95 (3')	45	15	200 (10')	good
9		95 (2')	6	Proximate (10um)	none		95 (3')	45	15	200 (10')	good
10		95 (2')	6	Proximate (15um)	none		95 (3')	45	15	200 (10')	good
11		95 (3')	6	Hard	none		110 (3')	45	15	200 (10')	good
11-A		95 (3')	6	Hard	none		110 (3')	45	15	150 (10')	not too good (see a gap between resist and substrate)
12		110 (3')	6	Hard	none		110 (3')	60	15	200 (10')	good
13		95 (3')	9	Hard	yes		95 (3')	60	15	200 (10')	good

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Figure 1 SU-8-2005 Resist Profile of Sample#04 (expose=6s). (a) and (b) Before O_2 Etch; (c) and (d) After O_2 etch, RIE5, for 15 minutes.

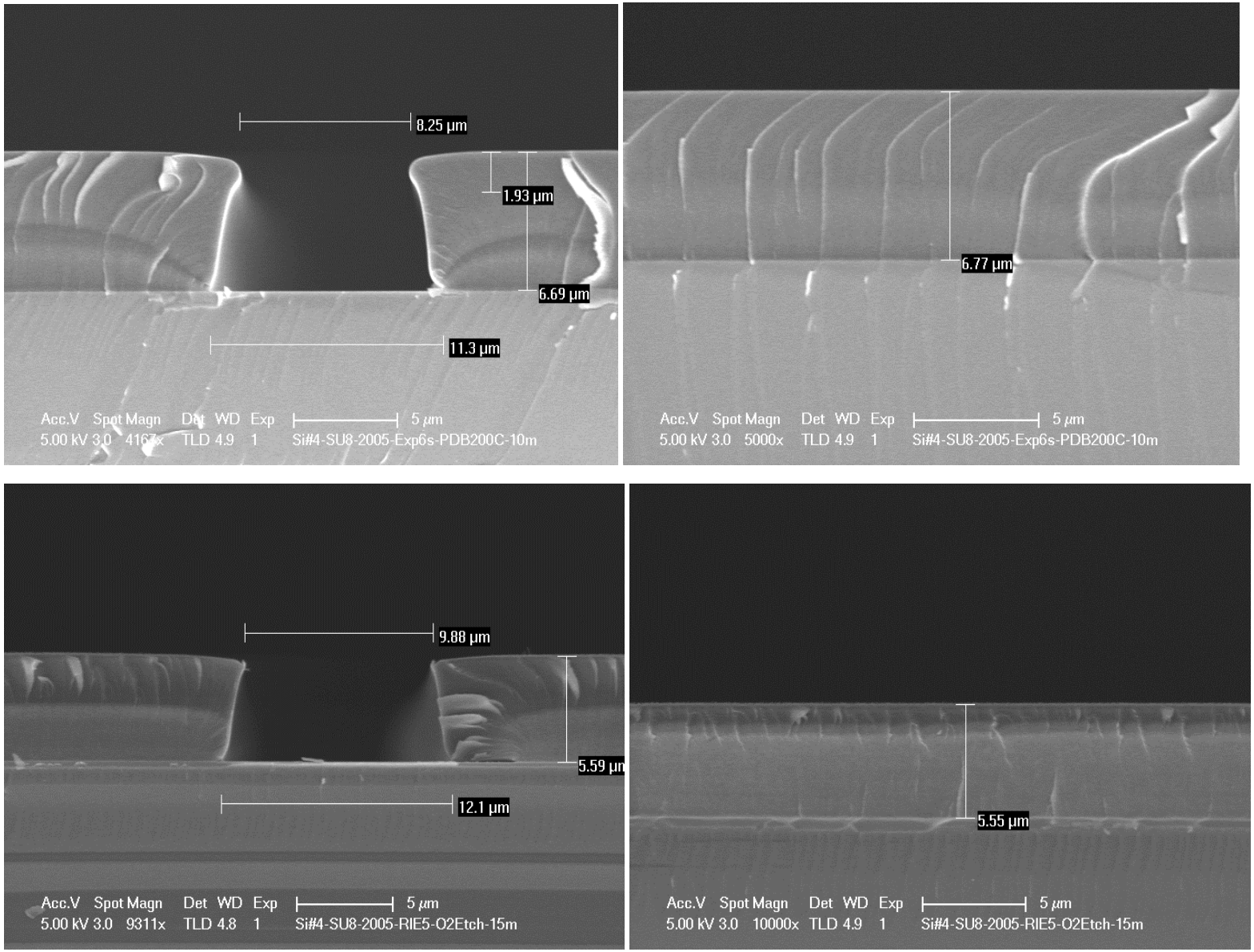

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Figure 2 SU-8-2005 Resist Profile of Sample#05 (expose=9s). (a) and (b) Before O_2 Etch; (c) and (d) After O_2 etch, RIE5, for 15 minutes.

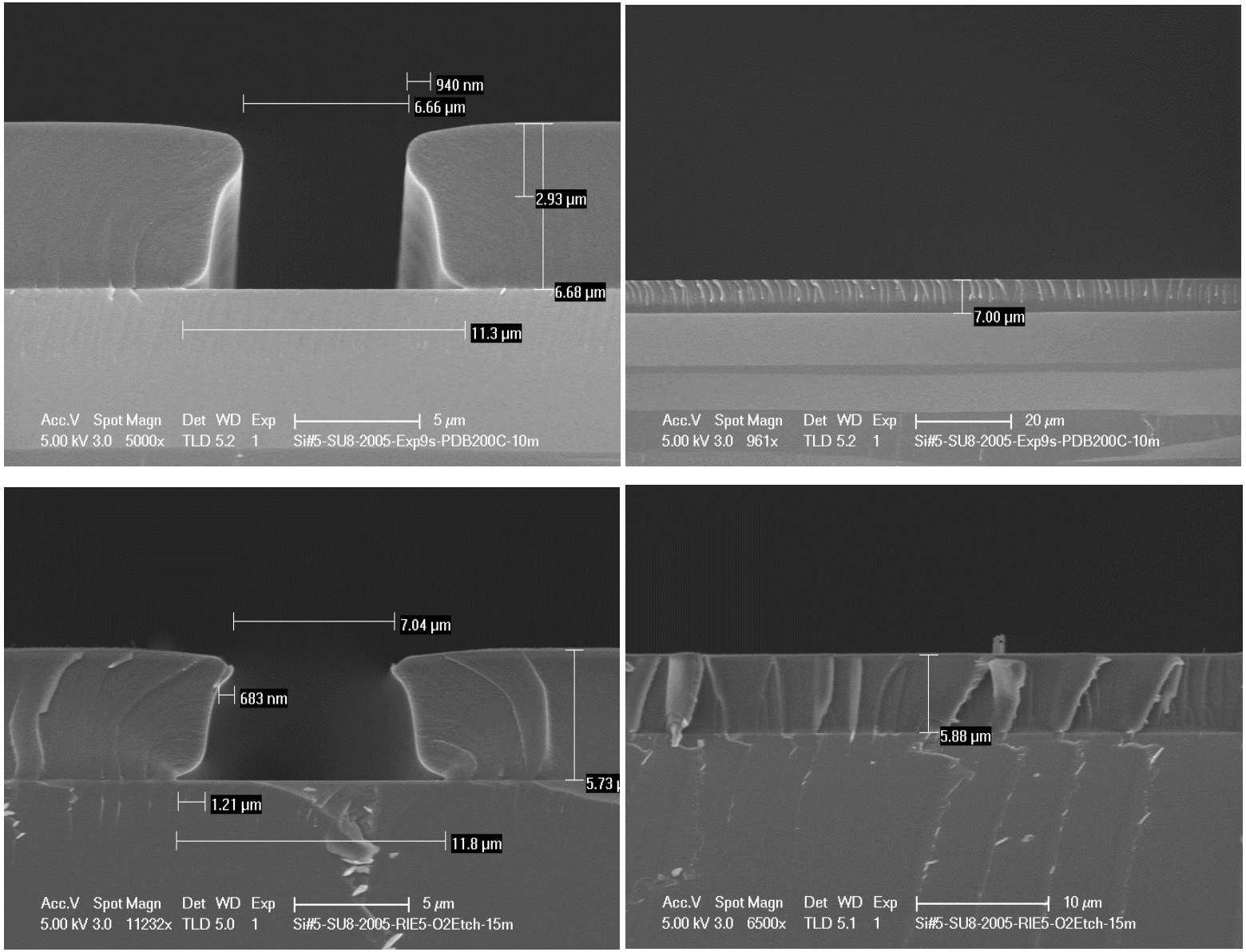

Figure 3 SU-8-2005 Resist Profile of Sample#06 (expose time=4 s).

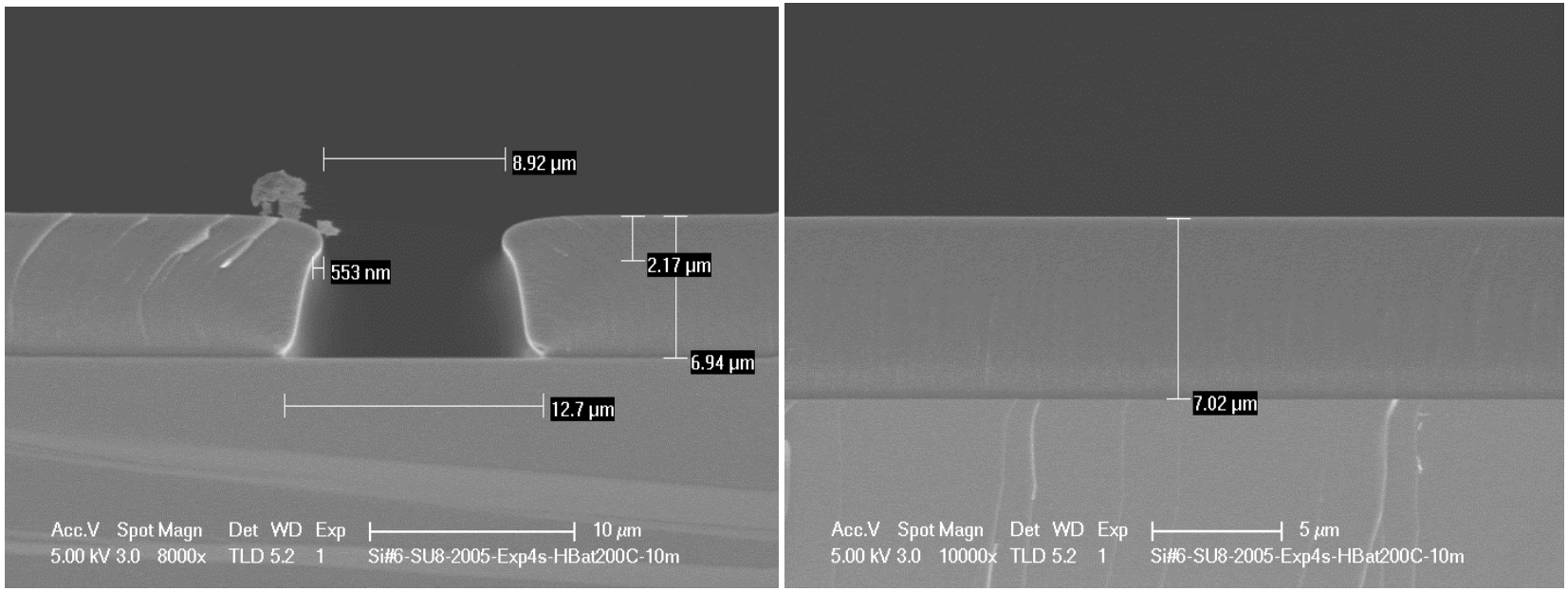

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Figure 4 SU-8-2005 Resist Profile of Sample#07 (expose time=5 s).

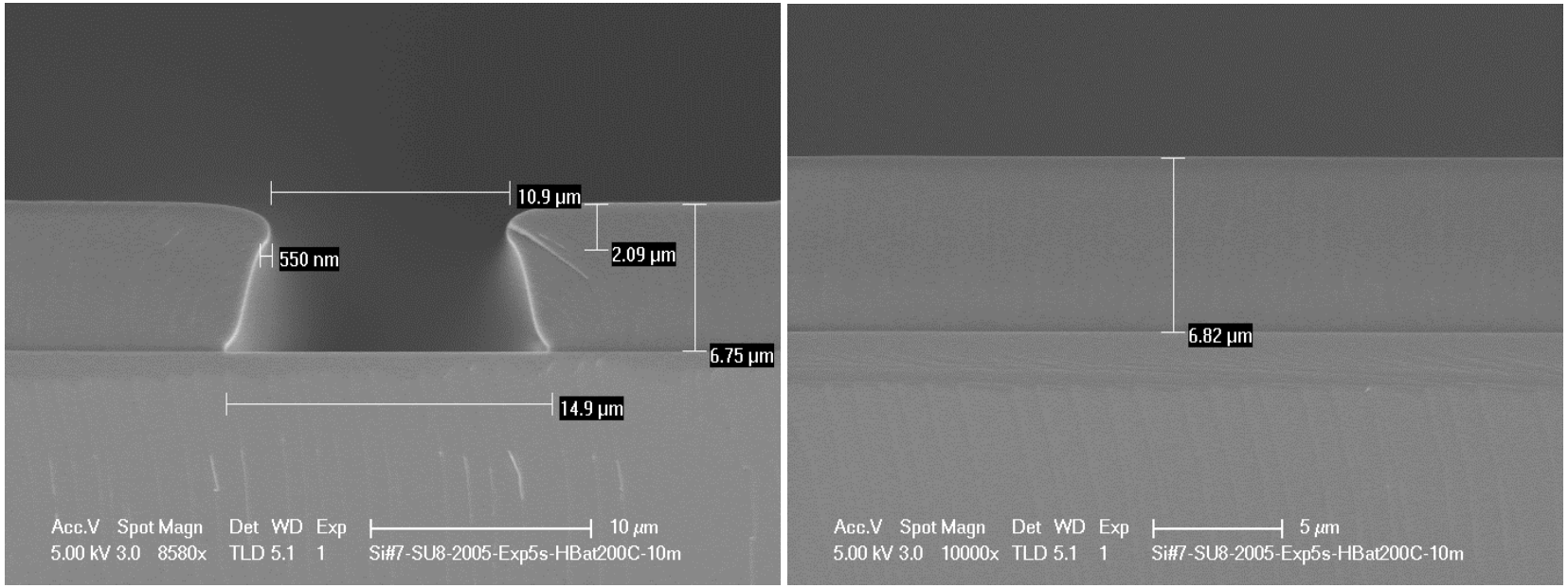

Figure 5 SU-8-2005 Resist Profile of Sample#08 (expose time=6 s).

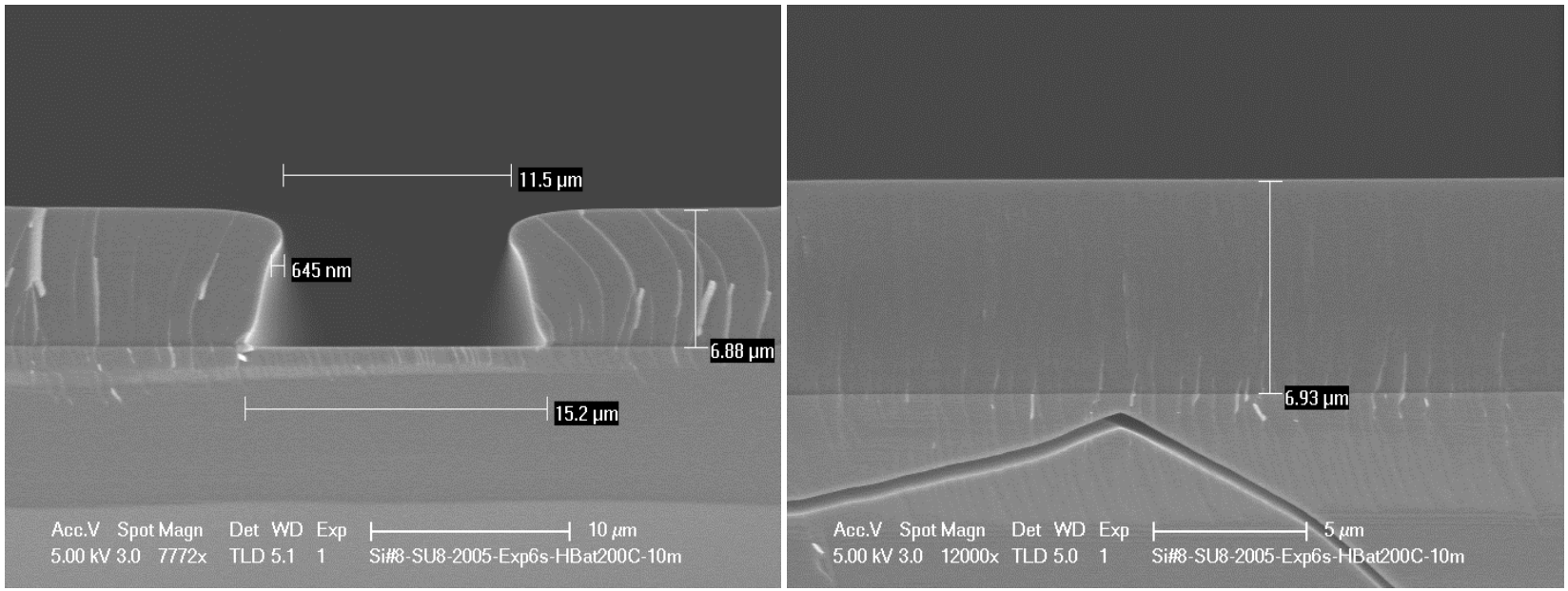

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Figure 6 SU-8-2005 Resist Profile of Sample#09 (proximate expose time=6 s and gap=10 μm).

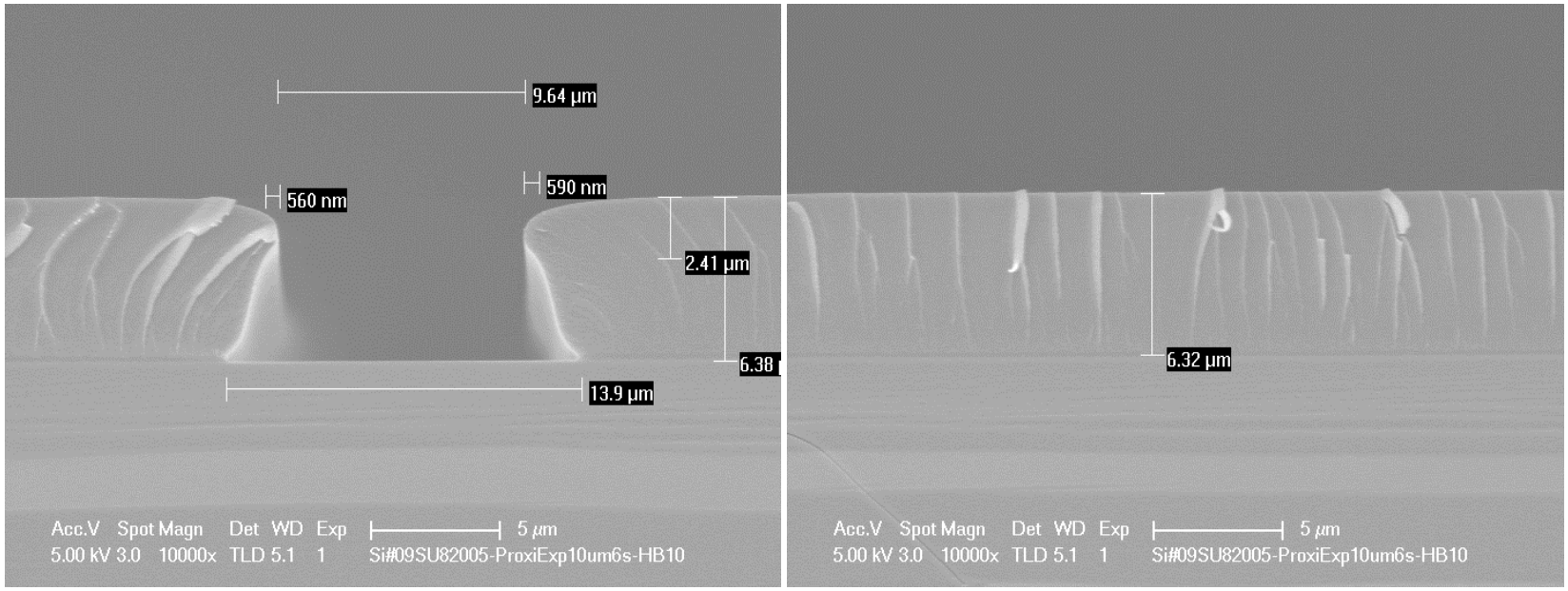

Figure 7 SU-8-2005 Resist Profile of Sample#10 (proximate expose time=6 s and gap=15 μm).

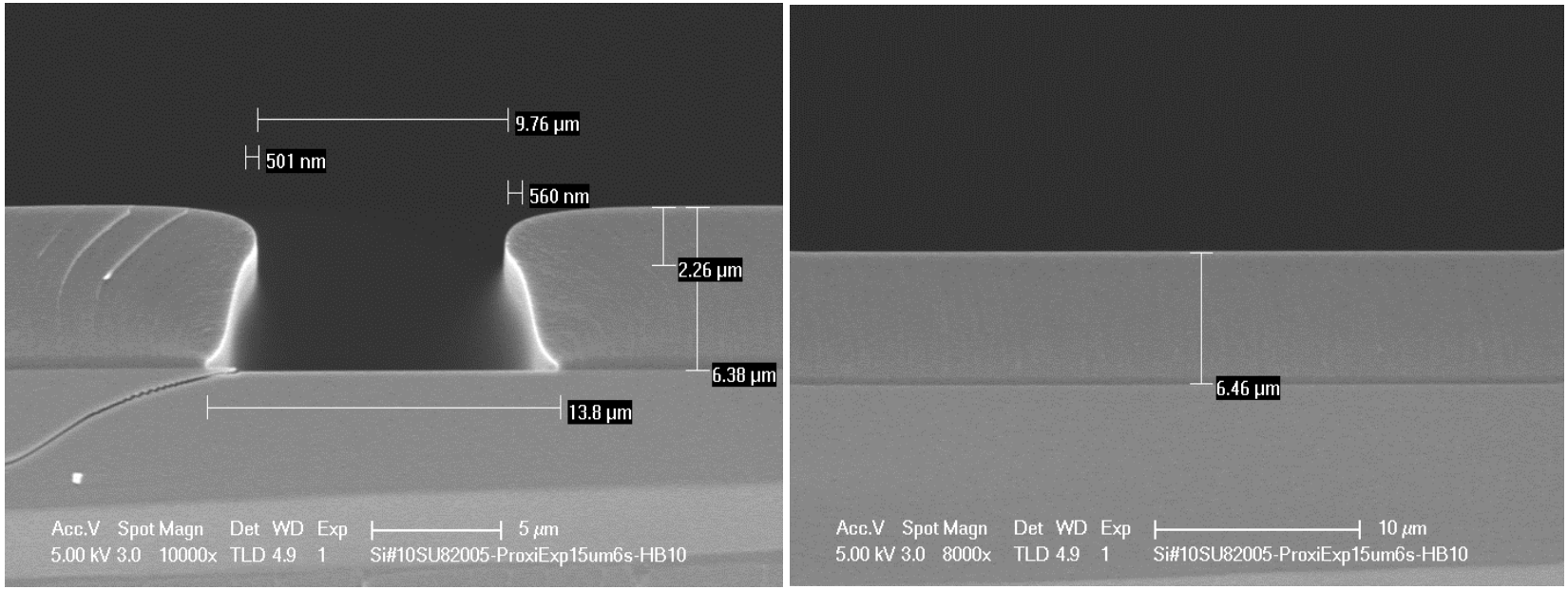

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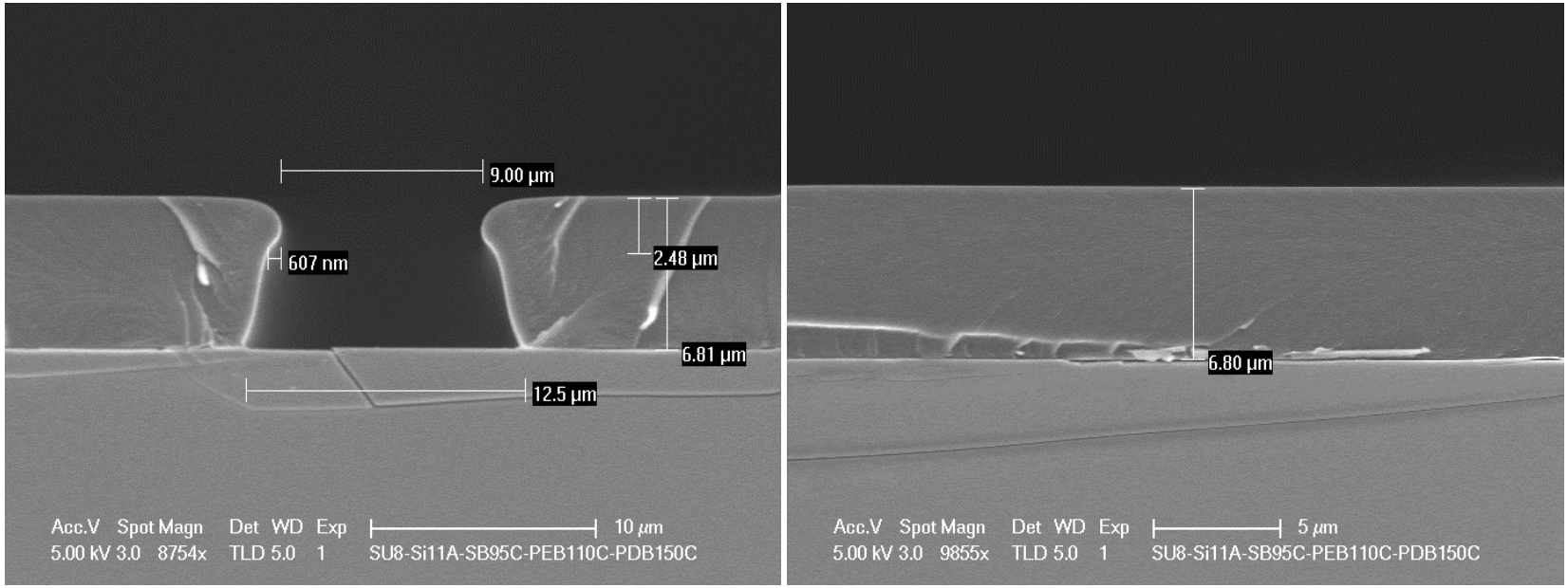
Figure 8 SU-8-2005 Resist Profile of Sample#11-A (expose time=6 s, soft bake at 95°C, post-exposure bake at 110°C, and post development bake at 150°C for 10 minutes).



Note: There is a gap between the resist and substrate which means the resist adhesion on Si substrate is not good.

Figure 9 SU-8-2005 Resist Profile of Sample#11 (expose time=6 s, soft bake at 95°C, post-exposure bake at 110°C, and post development bake at 200°C for 10 minutes).

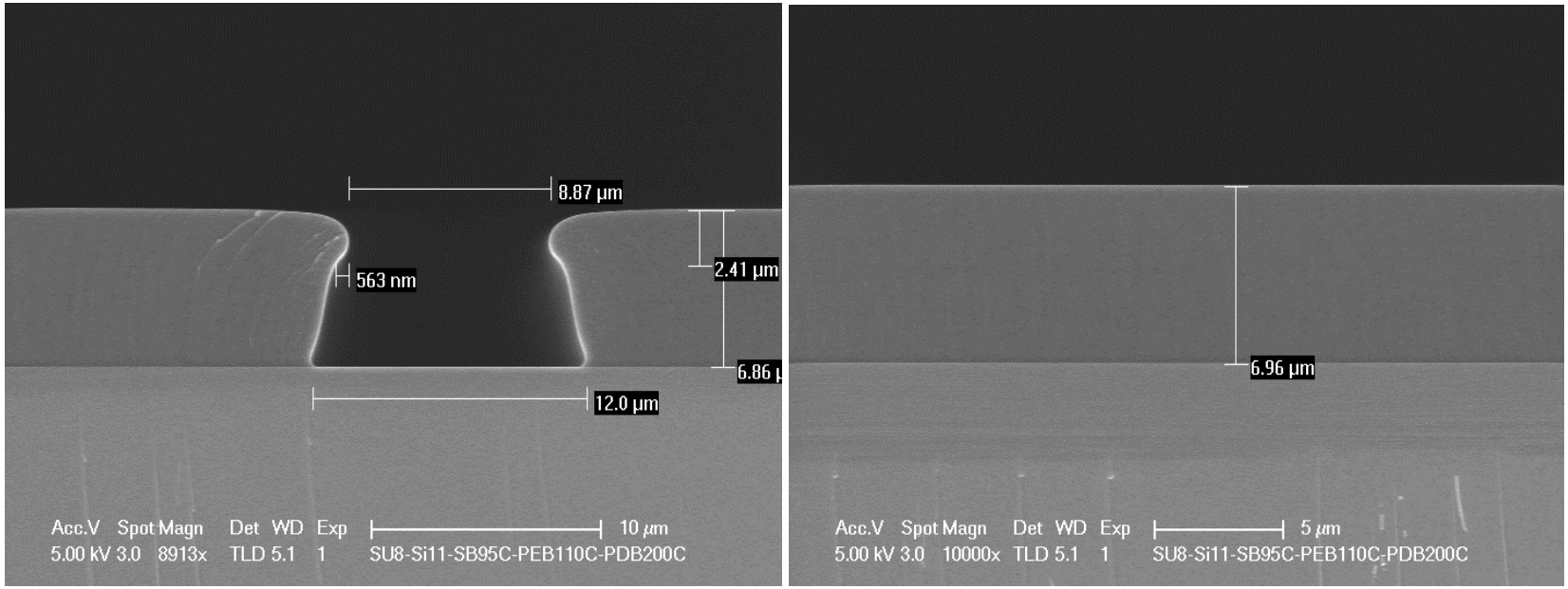
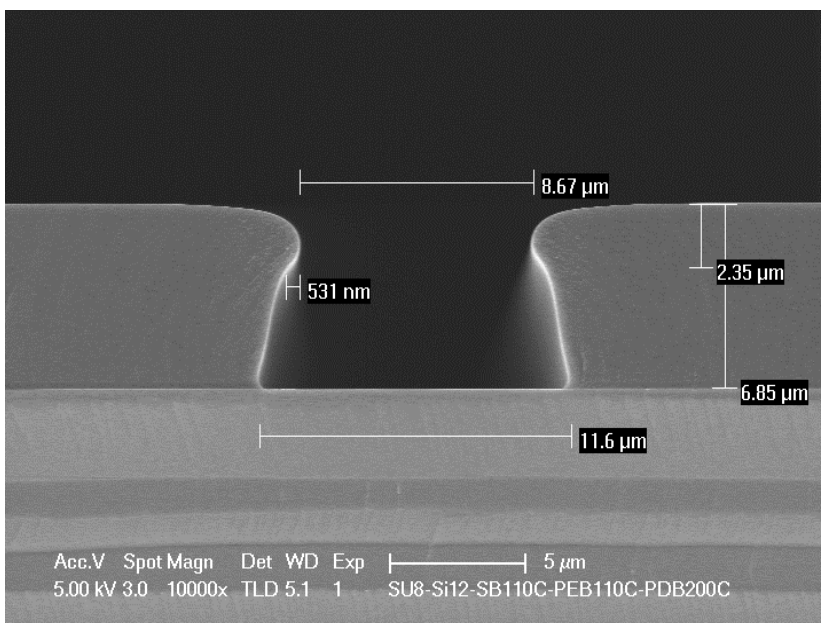


Figure 10 SU-8-2005 Resist Profile of Sample#12 (expose time=6 s, both soft and post-exposure bakes at 110°C, and post development bake at 200°C for 10 minutes).



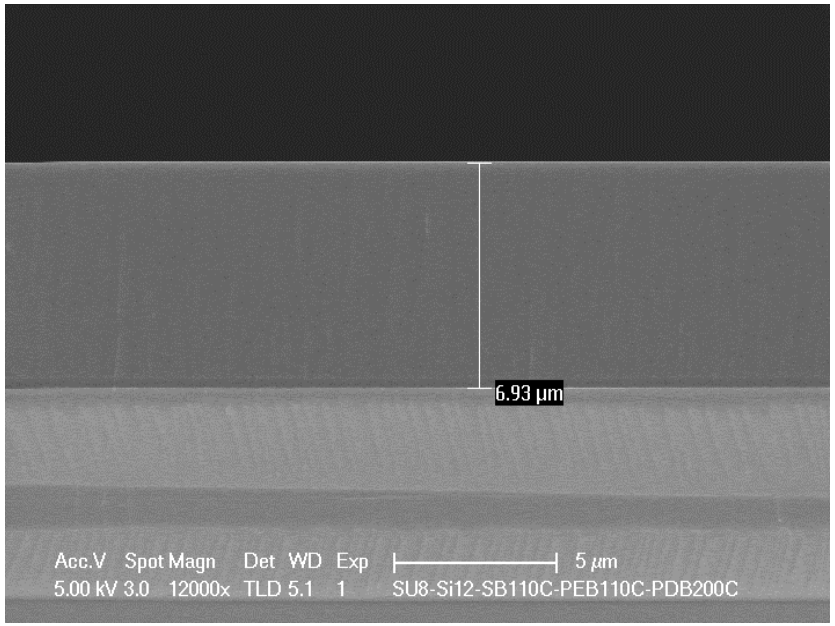


Figure 11 SU-8-2005 Resist Profile of Sample#13 (expose time=9 s, using UV filter, and post development bake at 200°C for 10 minutes).

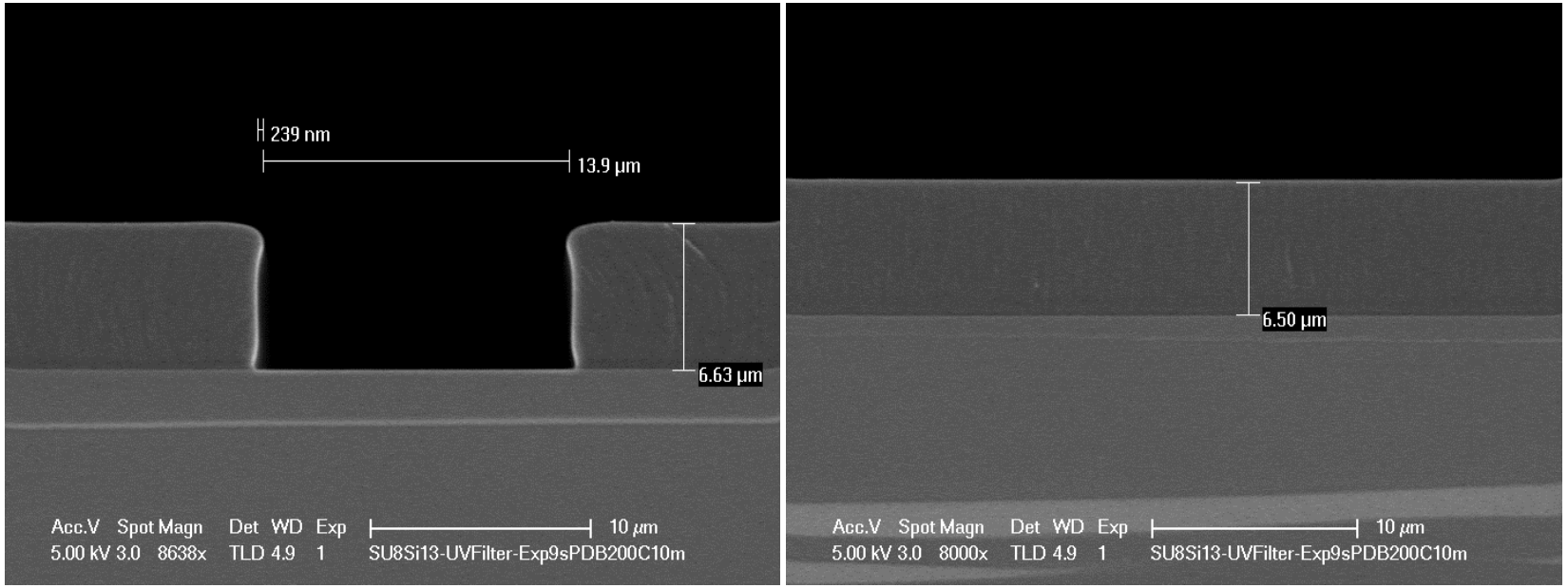
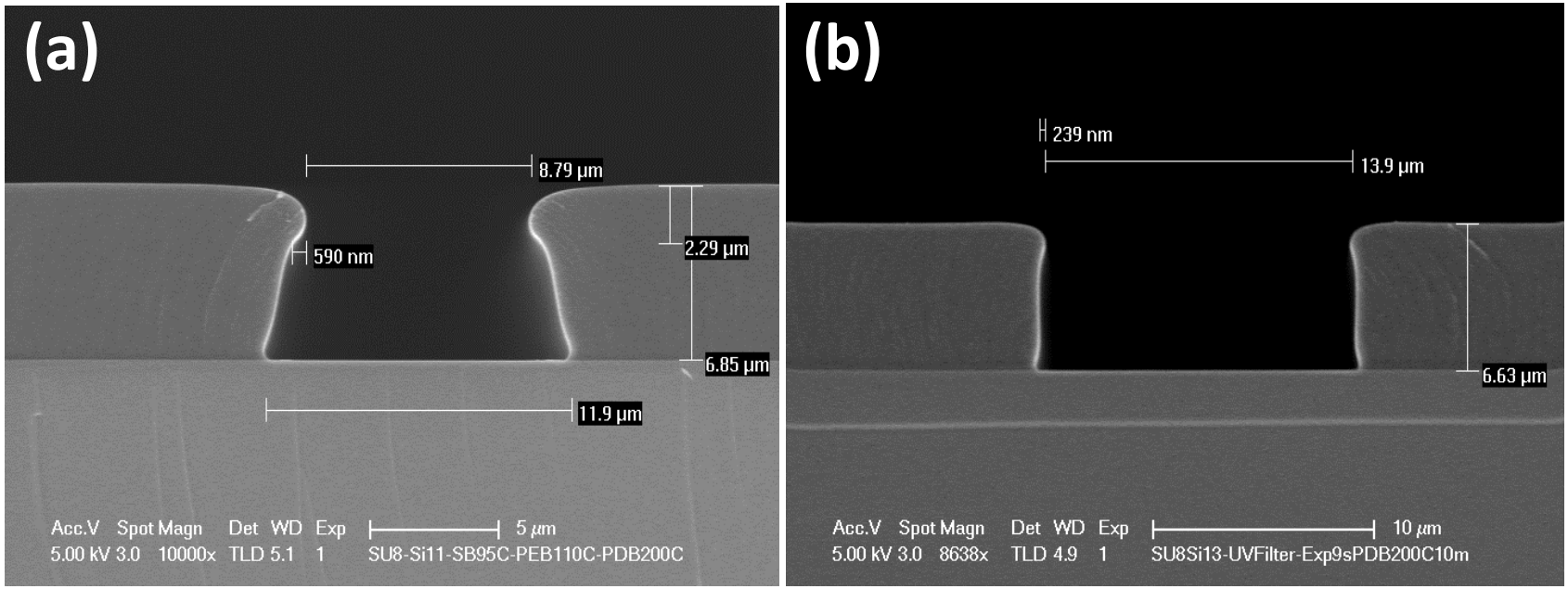


Figure 12 SU-8-2005 profile: (a) exposure time=6 s (without the UV filter); (b) exposure time=9 s (with the UV filter)



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Processing 2 mold wafers for FSU

1)Si wafers preparation: a) Soaking in acetone (2') and iso-propanol (2') in ultrasonic bath, then, nitrogen gas dry; b) Soaking in Nano strip tank at 70°C for 10 minutes, then, DI water rinse and nitrogen gas dry; c) Oxygen plasma treatment to make surface hydrophobic (PEII): 300mT/100 W for 30"; d) Dehydration bake at 200°C for 10 minutes (let it cool down on metal surface for 5 minutes).

2) Lithography:
a) Spin-on HMDS. 2500 rpm for 30".
b) Spin-on SU8-2005. Two steps: first one: 500 rpm with 100 rpm/s ramp for 8"; second one: 2500rpm with 300 rpm/s for 30".
c) Soft bake at 95°C for 3 minutes, then, let it cool down on cleanroom paper for 5 minutes.
d) Resist expose using MA-6 aligner, 2 masks (one is 7-μm in diameter holes; the other is 9 different hole-size pattern), and a UV Filter (HOYA UV-34[200-750nm]: cutting the transmission off by 50% at 350 nm).
f) Post expose bake at 95°C for 3 minutes, then, let it cool down on cleanroom paper for 5 minutes.
g) Development in SU8 developer: 1) for the 7-μm hole pattern, in the first developer bath for 80", then, in the second fresh developer bath for 20" in ultrasonic bath, then, rinse the sample with isopropanol and soak in isopropanol for 30", then, nitrogen gas dry (with a low pressure, less than 20 psi); 2) for the 9 different hole-size pattern, in the first developer bath for 70", then, in the second fresh developer bath for 20", then, rinse the sample with isopropanol and soak in isopropanol for 30", then, nitrogen gas dry (with a low pressure, less than 20 psi);
h) Post development bake at 200°C for 15 minutes with a glass cover, then, let it cool down on paper for 5 minutes (to improve the resist adhesion on Si substrate).

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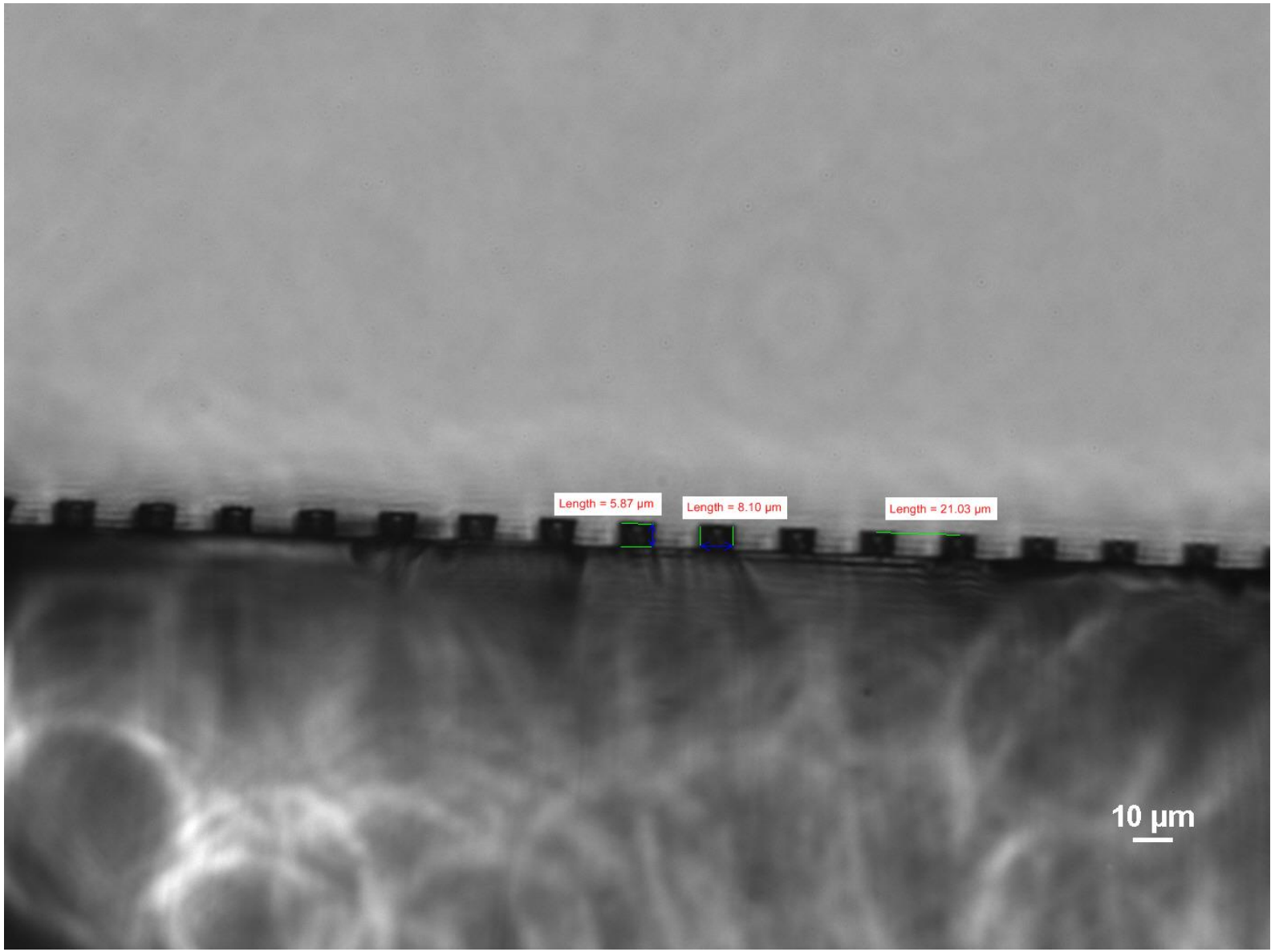
Figure 13 PDMS casting using the SU-8 mold wafer.



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