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Very-Low Pin-Hole-Density SiN_x Film Deposited at 300 C using Unaxis HDPCVD Tool

Purpose: One of our external customers requested us to grow a high quality SiO_2 (1 μm)/SiN_x (0.2 μm)/SiO_2 (1 μm)/SiN_x (0.2 μm) multi-layer film on a Cr-patterned Si wafer using our Unaxis high-density-plasma CVD (HDPCVD) tool for him. This Unaxis deposition tool is partially different from a conventional PECVD tool by the facts that (1) the wafer chuck is severed as a cathode so that, during the deposition run, the ions in the plasma bombard the wafer surface which can cause pin-holes in the growing film if the bias power is too high; (2) Intrinsically, the stress of the SiN_x is very high, resulting in a crack film under a small bias power, *e.g.*, ~1.8 GPa in compression at a bias power of 5 W and a chuck temperature of 250 C, and the only way to reduce the stress is to apply a higher bias. So, there is a conflict of interest between a low stress and a low pin-hole density of the SiNx film deposited using this tool. Here, to meet this customer's need, it is required to find a compromised bias power, under which the SiNx film is not crack and is pin-hole free.

Experimental:

The SiNx deposition tests were carried out in the following condition: 15mT, 25 (bias)/400 (ICP) W, SiH_4/N_2/He/Ar flow-rate=7.2/4/350/20 SCCM, chuck temperature=300 C, and time=300 s (550 s for the film on a 4" Si wafer for the stress and KOH pin-hole tests).

Result:

1) Deposition Rate=212 Å/min;

2) Reflective Index=2.01;

3) Buffered HF Etch Rate=400 Å/min;

4) Film Stress (at a thickness of 1944 Å) =-893 MPa.

5) Pin-Hole test was carried out with the film wafer being soaked in a heated KOH at 90 C for 32.5 minutes. The result shows (see Figure 1) there is almost no pin-hole in the film.

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Figure 1 Pin-hole test result after the SiN_x film (1944 Å in thickness) wafer being in the hot (90 ^oC) KOH for 32.5 minutes. Note: there are some pin-holes in the film, which were caused by some small particles on the test-graded Si wafer prior to the deposition.

Next thing was to grow a SiO_2 (1 μm)/Si_3N_4 (0.2 μm)/SiO_2 (1 μm)/Si_3N_4 (0.2 μm) multi-layer film on the customer-supplied Cr-patterned Si wafer. The deposition sequence was 1) cleaning the process-module-3 (PM3) deposition chamber with SF_6/O_2/Ar plasma and doing SiO_2 chamber season; 2)transferring the customer's wafer from load-module (LM) to the PM3 and growing the first SiO_2 and Si_3N_4 layers, then, transferring the wafer from PM3 to LM (LM was still under a lower vacuum); 3) cleaning PM3 and doing SiO_2 chamber season again; 4) transferring the wafer from LM to PM3 and growing the second SiO_2 and Si_3N_4 layers. The result (see Figure 2) shows the film is good: there is no cracking in the film.

Figure 2 (a) and (b) Microscopic pictures of the SiO_2 (1 μm)/Si_3N_4 (0.2 μm)/SiO_2 (1 μm)/Si_3N_4 (0.2 μm) multi-layer film, deposited using Unaxis HDPCVD tool at a chuck temperature of 300 ^oC on the customer's Cr-patterned wafer. The deposition condition of Si_3N_4 was 15mT, 25/400W, SiH_4/N_2/He/Ar flow-rate=7.2/4/350/20 SCCM, and time=566 seconds; the deposition condition of SiO_2 was 5mT, 15/800W, SiH_4/O_2/Ar flow-rate=27.5/55/20 SCCM, and time=540 seconds.