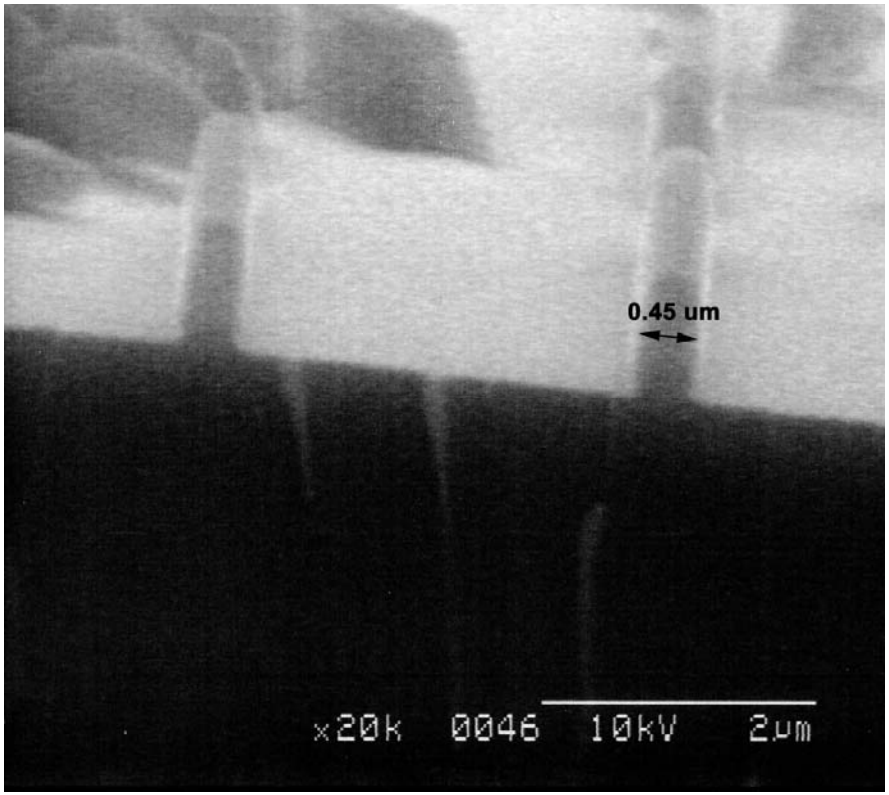
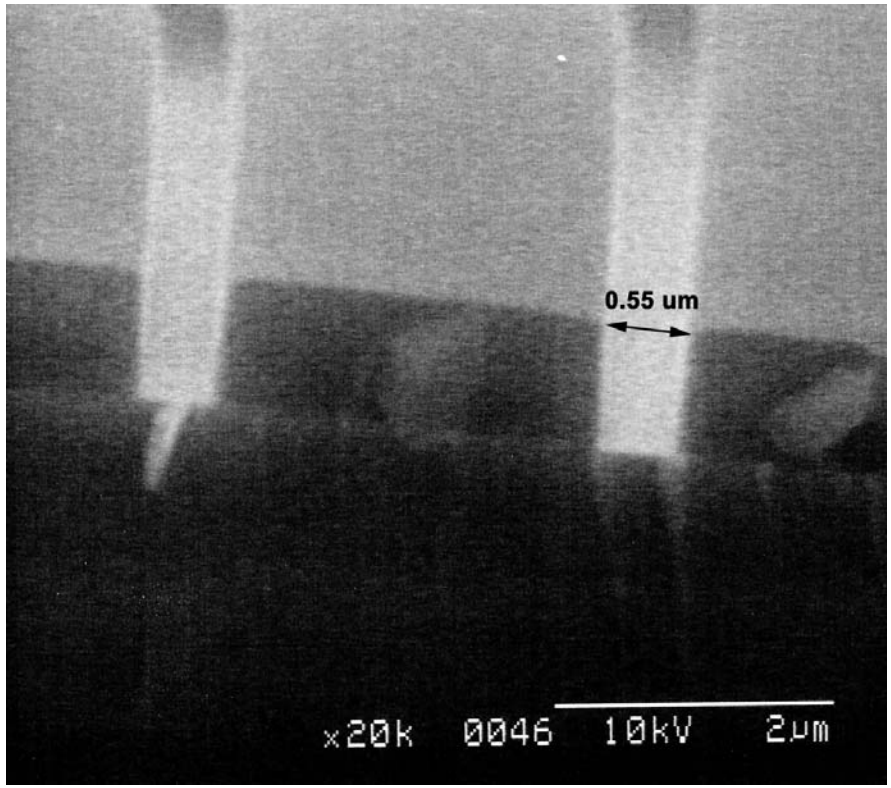
SPR955CM-0.9

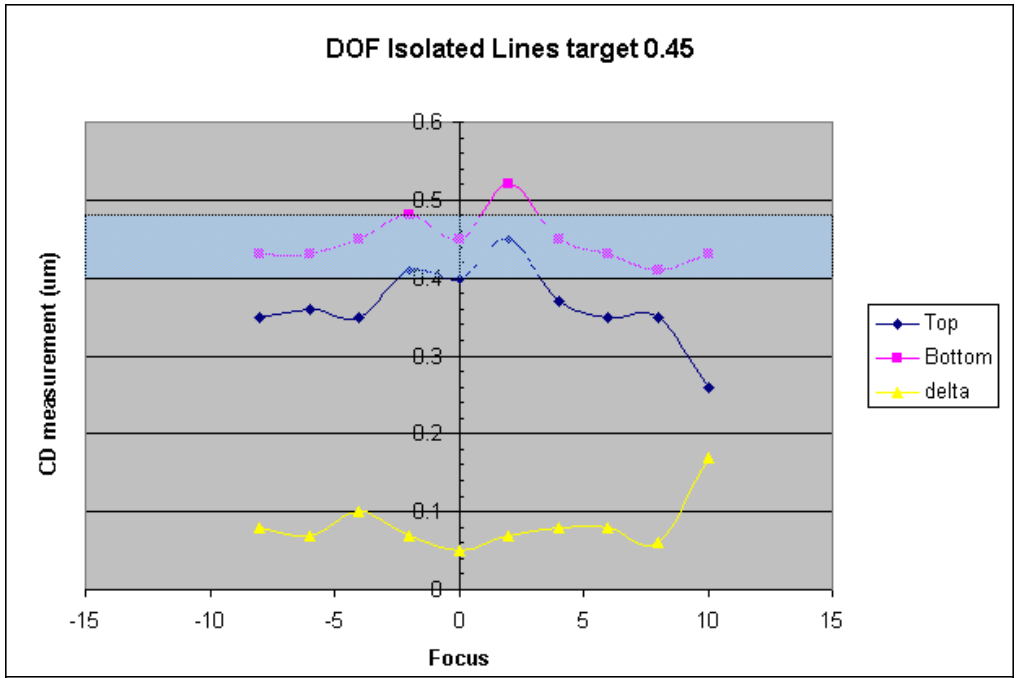
Standard Recipe
With CEM Top Layer
Small Contact Holes
Silicon Wafer

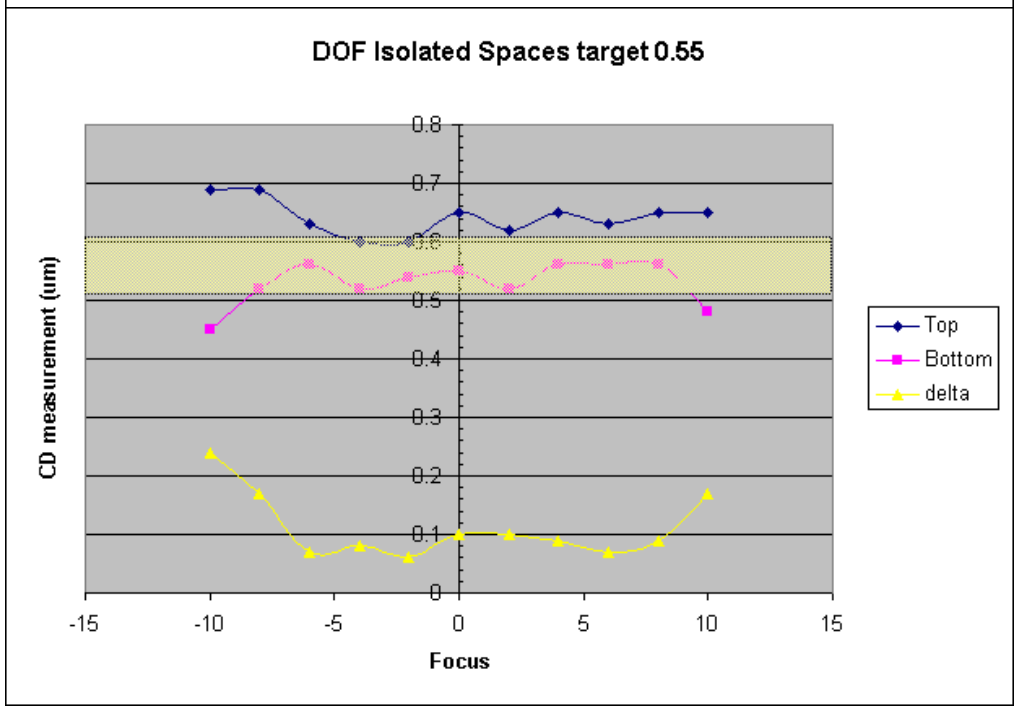
Standard Recipe



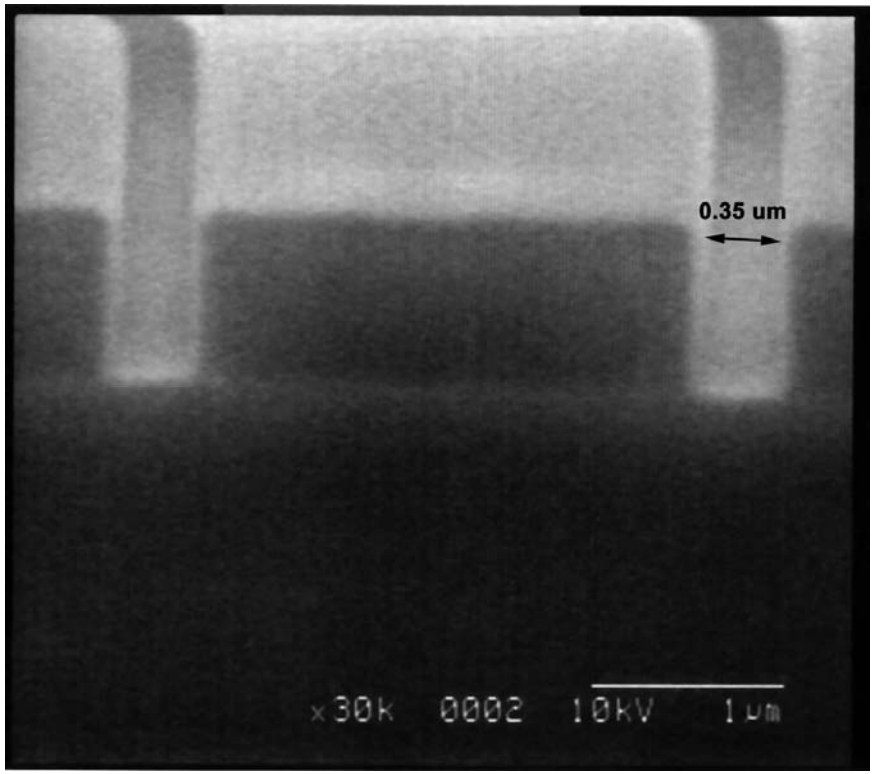


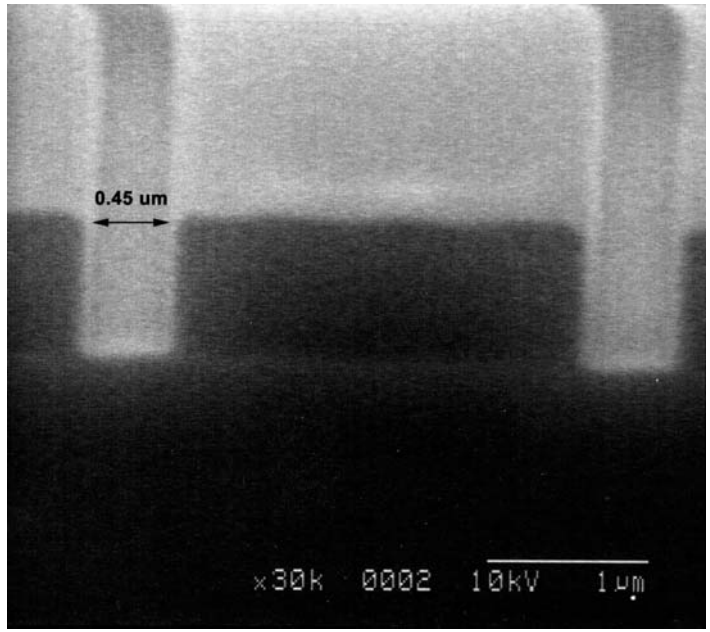
HMDS
3000rpm/30”
95 C/ 60” Soft-Bake
Expose 1.1”, Focus Offset 0 (optimum)
110 C/ 60” PEB
MF701 60” Develop

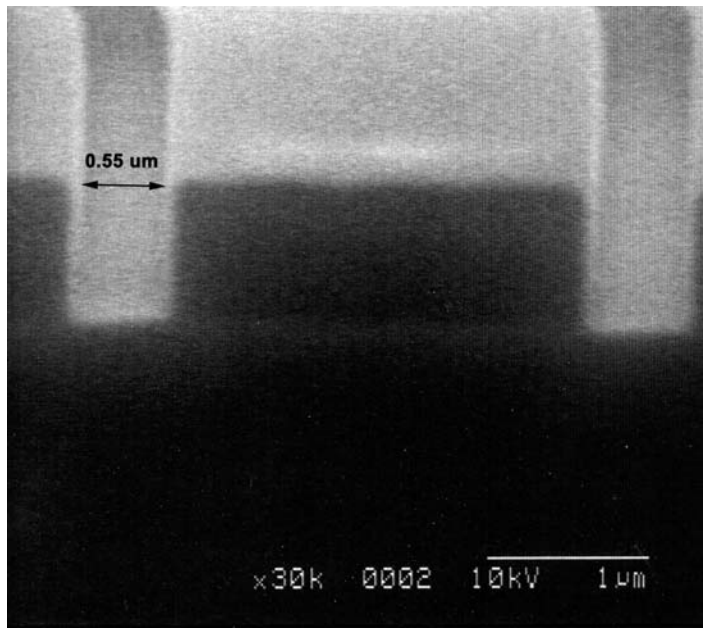

DOF Isolated Lines target 0.45
CD measurement (um)
0.6
0.5
0.4
0.3
0.2
0.1
0
-15
-10
-5
0
5
10
15
Focus
Top
Bottom
delta


DOF Isolated Spaces target 0.55
CD measurement (um)
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
-15
-10
-5
0
5
10
15
Focus
Top
Bottom
delta

With CEM top layer

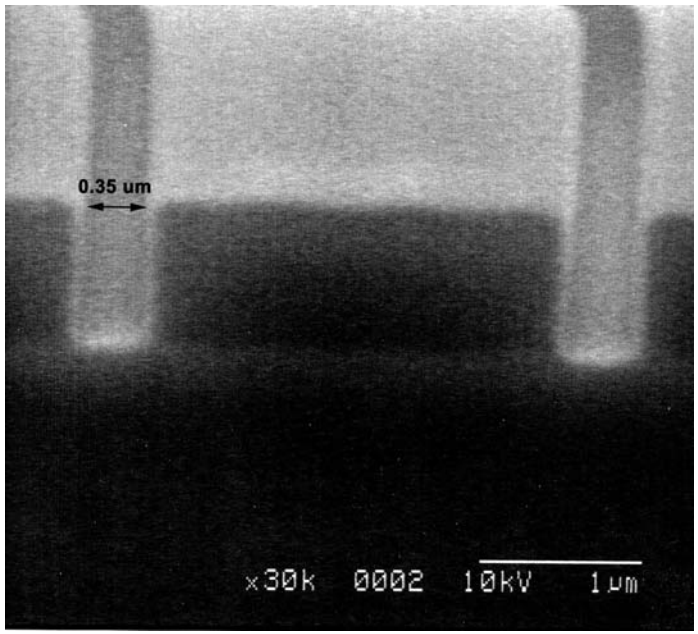




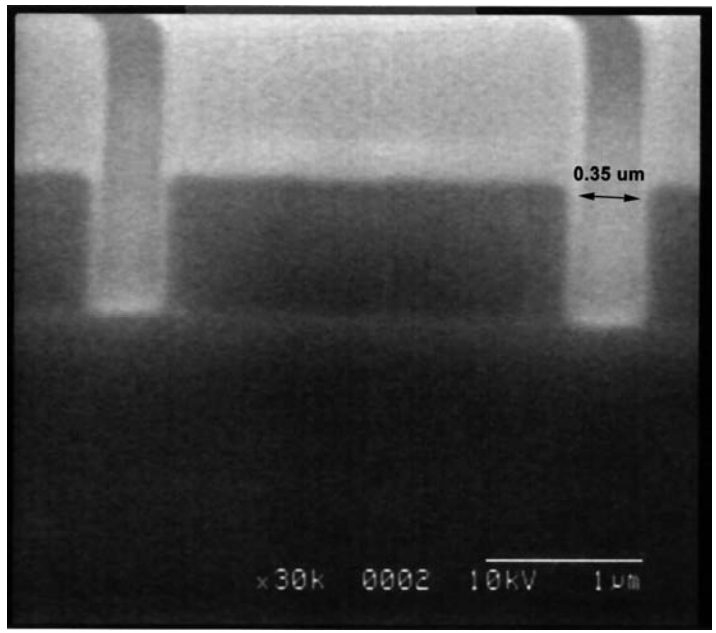


HMDS
3000rpm/30”
95 C/ 60” Soft-Bake
CEM365iS 5000rpm/30”
Expose 2.2”, Focus Offset -10 (optimum)
DI Rinse
110 C/ 60” PEB
MF701 60” Develop

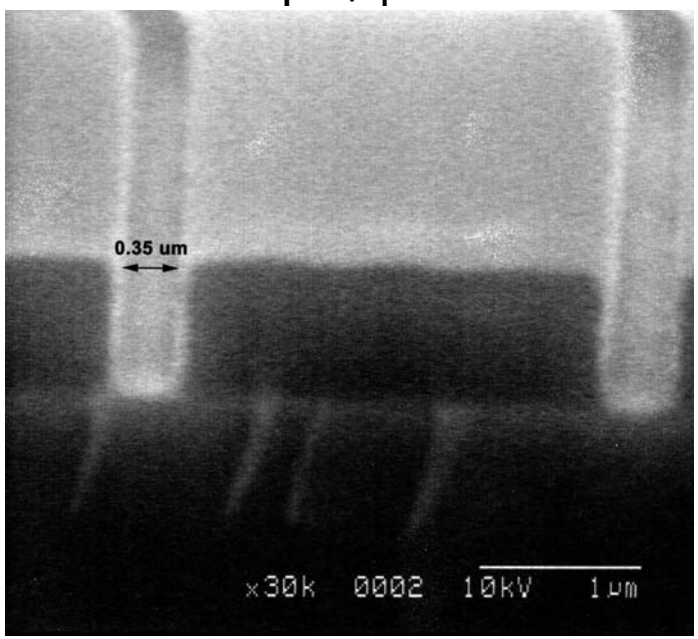
F=-4

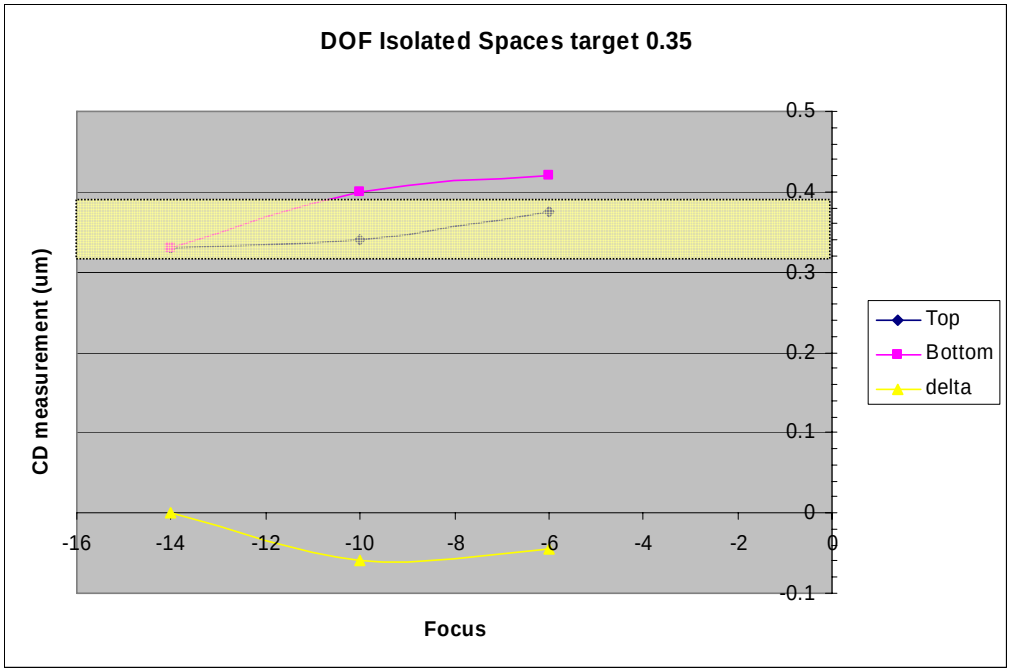

0.35 um
x30k 0002 10kV 1 um

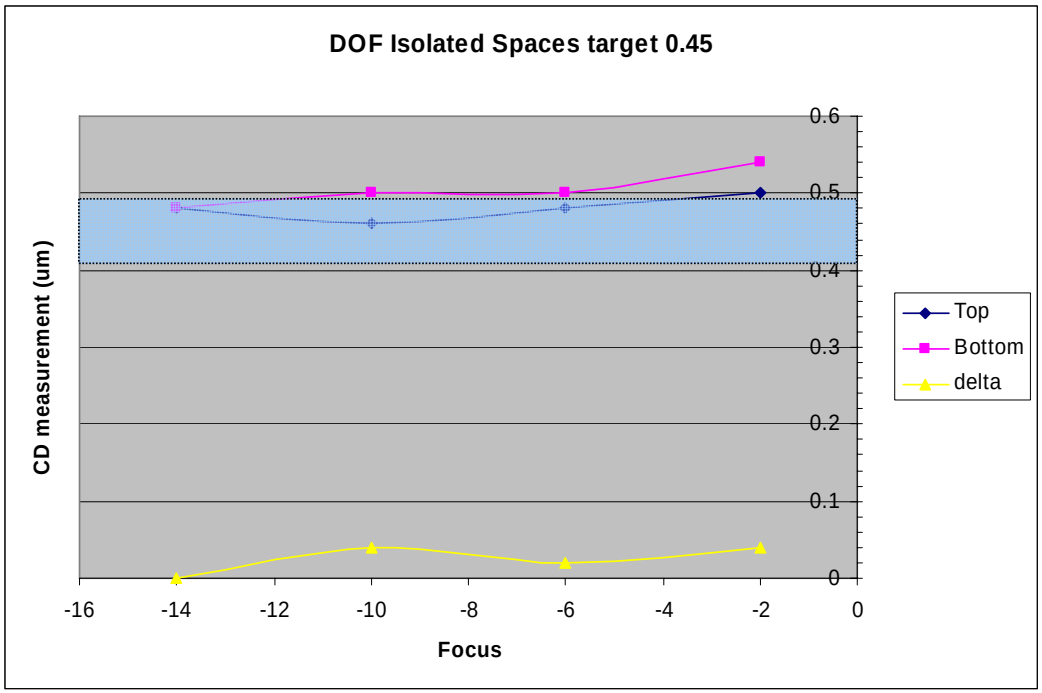
F=0


0.35 um
x30k 0002 10kV 1 um

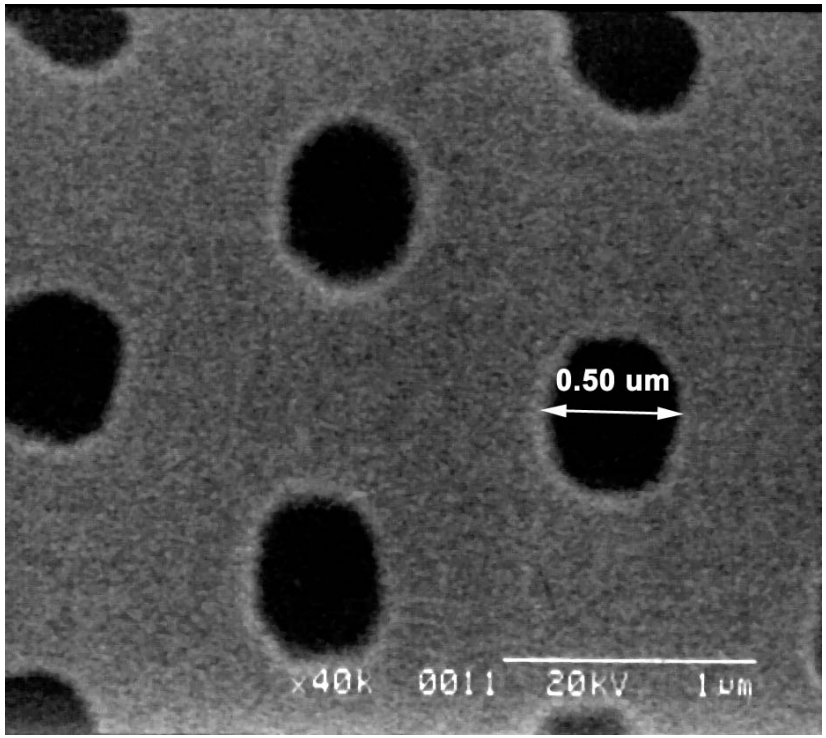
F=+4


0.35 um
x30k 0002 10kV 1 um


DOF Isolated Spaces target 0.35
CD measurement (um)
0.5
0.4
0.3
0.2
0.1
0
-0.1
-16
-14
-12
-10
-8
-6
-4
-2
0
Focus
Top
Bottom
delta


DOF Isolated Spaces target 0.45
CD measurement (um)
0.6
0.5
0.4
0.3
0.2
0.1
0
-16
-14
-12
-10
-8
-6
-4
-2
0
Focus
Top
Bottom
delta

Small Contact Holes (on SiO2 film)



HMDS
3000rpm/30”
95 C/ 60” Soft-Bake
Expose 3.0”, Focus Offset 4 (optimum)
110 C/ 60” PEB
MF701 60” Develop