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Reducing Silicone Nanowire Diameter by Thermal Oxidation and Vapored HF Etch

Motivation: Silicone nanowire created using Holography has a diameter of ~100 nm. In some applications, researchers need to further decrease the size of these nanowire. In this study, I will show a relative easy way to reach this goal.

Experiment:

A) Holography

1) Cleaning SiO_2 (~200 nm)/Si sample (1x1 $inch^2$) with acetone (2min.) and methanol (1min.) in ultrasonic bath, then, DI-water rinse and

N_2 blow-dry

2 Dehydration at 115C for 10 min.

3 Spin-on XHRiC-11 (ARC: anti-reflectance-coating) at 2000 rpm for 40 sec.

4 Bake at 175 C for 60 sec.

5 Waiting for 2 min.

6 Spin-on THMR-IP3600HP-D resist at 5000rpm for 30 sec.

7 Bake at 90 C for 90 sec.

8 Exposing the resist with an energy dose of 55mJ (twice for 2D-dot pattern with the sample orientation rotated 90^o)

9 Post-exposure-bake (PEB) at 115 C for 120 sec (then, waiting for 2 min.)

10 Developing the resist in AZ300MIF developer for 12 sec, then, DI-water rinse (small DI water flow) and N_2 blow-dry (small gun pressure, less than 20 psi)

11 O_2 plasma descum with 300mT/100W for 20sce.

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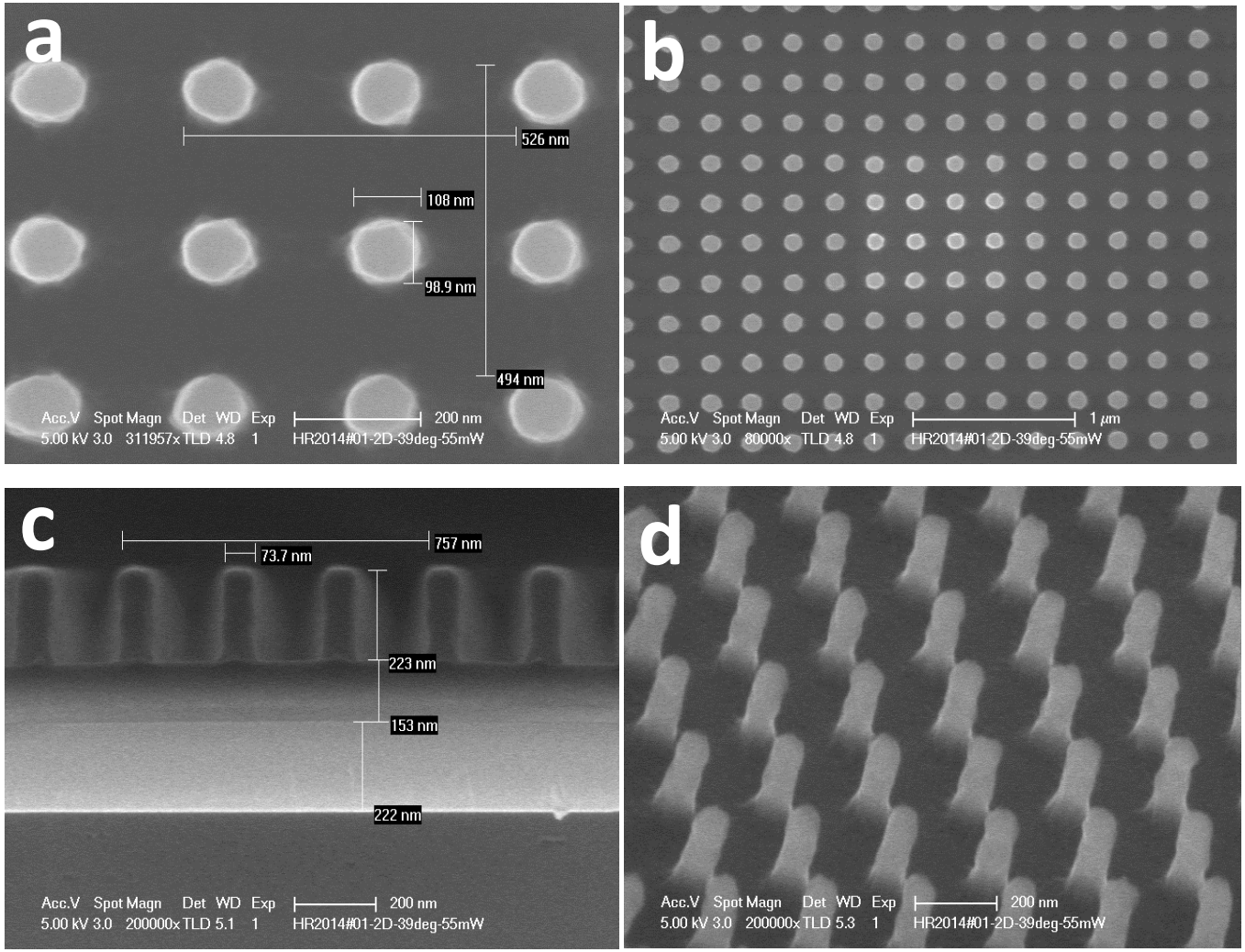
Figure 1. 2D-dot resist pattern after Holography. a) top view; b) another top view; c) cross-section view; d) 45^{o} view.



B) Etching XHRiC-11 (ARC) Layer using RIE#5

1) Cleaning RIE#5 etch chamber with O_2 plasma (8 mT, 200 W, O_2=20sccm, and 30 minutes).

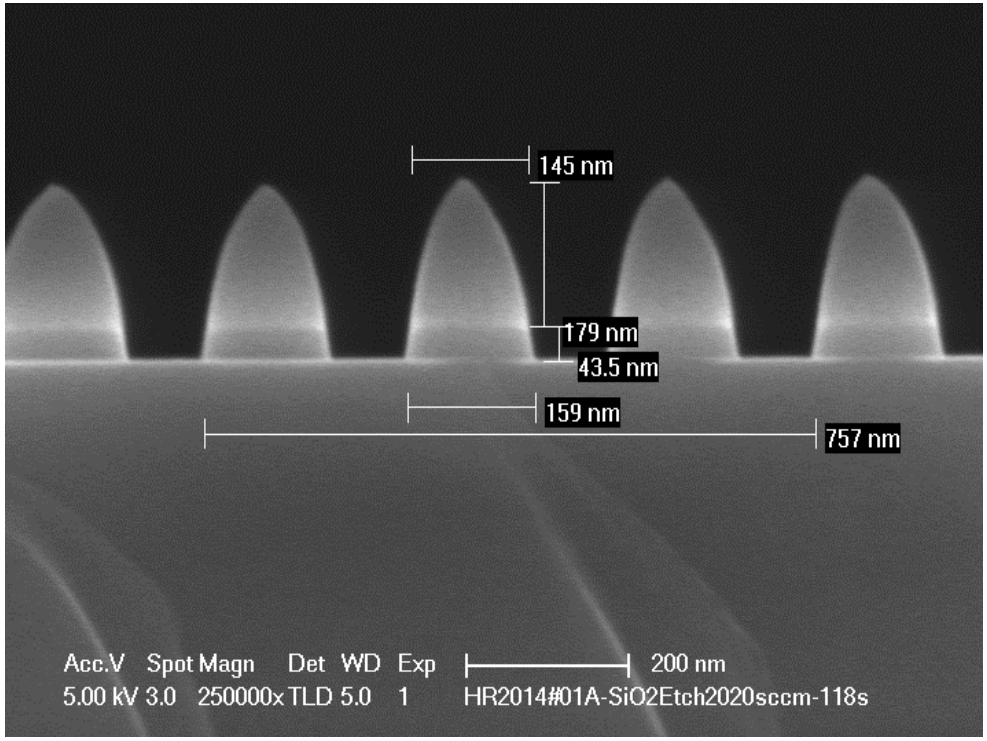
2) Etching ARC with 5 mT, 150 W, O_2=20sccm, and 140 sec.

C) Etching SiO_2 Layer using Panasonic ICP#2

1) Cleaning ICP#2 etch chamber with O_2 plasma for 30 minutes.

2) Etching SiO2 with 0.5 Pa, 50/900 W, CF4/CHF3=20/20 sccm, and 118 sec.

Figure 2. Cross-section profile after etching SiO2 with 0.5 Pa, 50/900 W, CF4/CHF3=20/20 sccm, and 118 sec.



Note: The SiO2 was over-etched into Si as seen in above figure.

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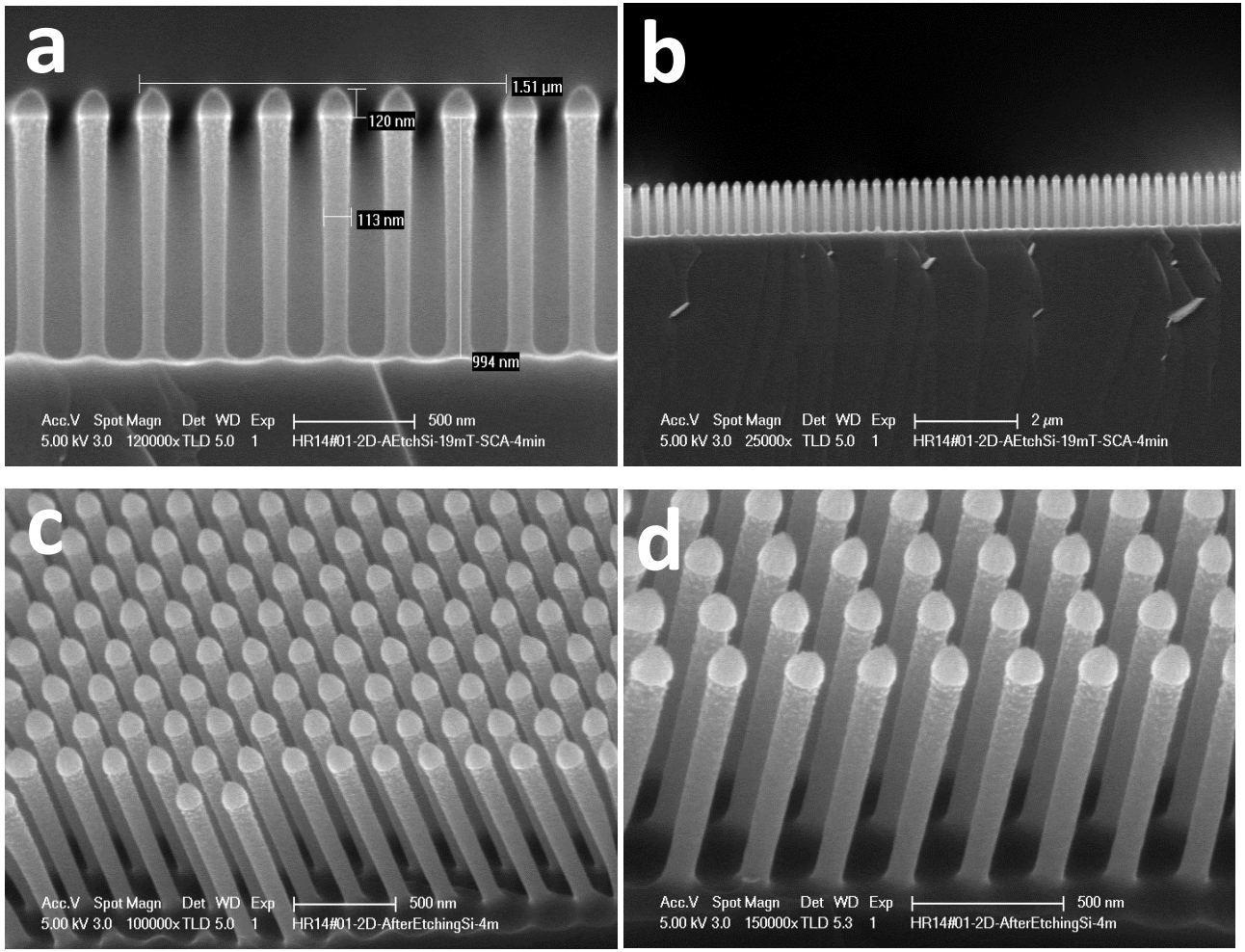
D) Etching Si nanowire using DRIE Etch Tool

1) Cleaning DRIE etch chamber with O_2 plasma for 30 minutes.

2) Etching Si with 19mT, 15/800 W, C4F8/SF6/Ar=54/26/20 sccm, and 4 minutes.

Figure 3. Etched Si nanowire profile. a) and b) cross-section; c) and d) 45 degree view.



The average diameter of Si nanowire is 106.8 nm

To reduce the size of nanowire, the nanowire sample was put into the Tystar thermal oxidation furnace for certain period of time (got the time from an internet site, http://www.cleanroom.byu.edu/OxideTimeCalc.phtml, found by Tony Bosch, an engineer of our Lab), Then, put the oxidized sample into Vapored HF tool to etch the oxide off Si substrate.

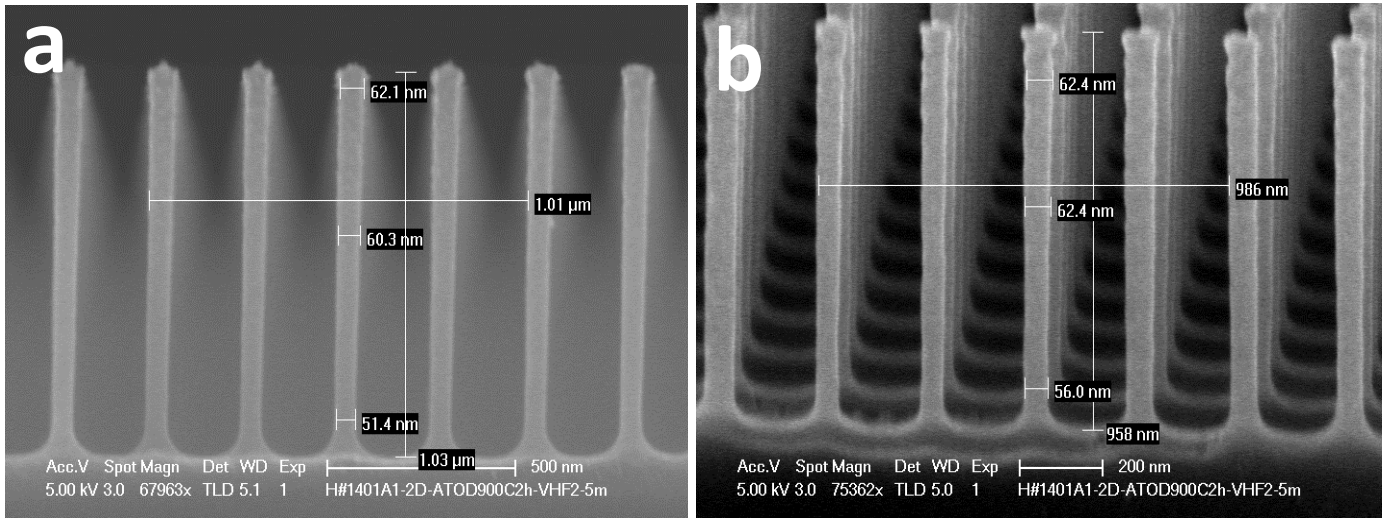
1) Test#1

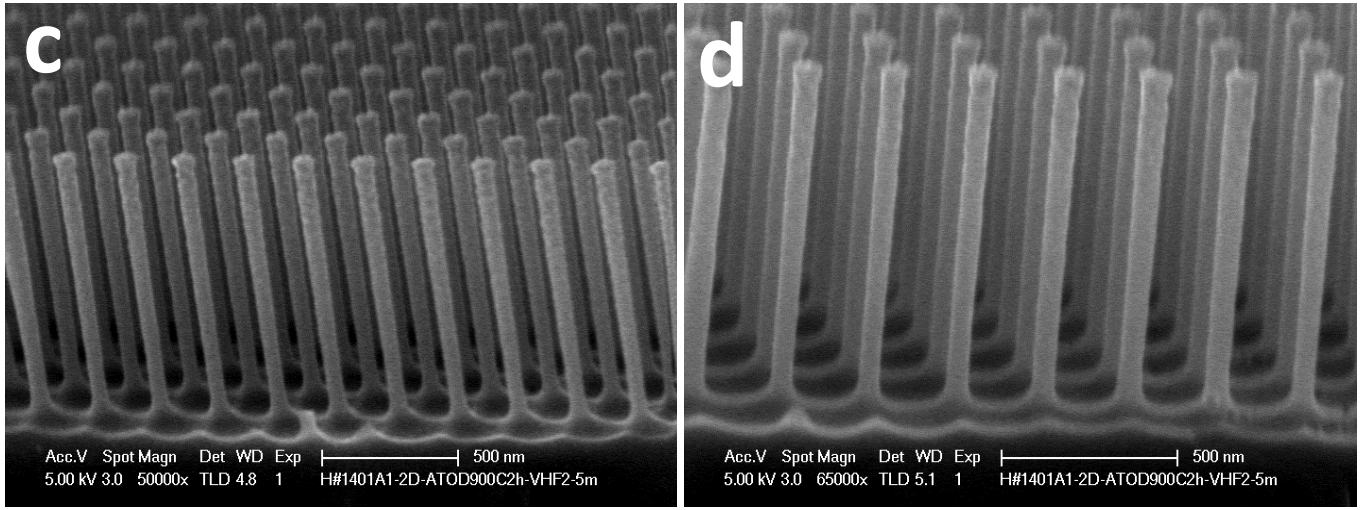
The target SiO2 layer thickness=20 nm: Dry thermal oxidation was carried out at a temperature of 900 C and time of 2 hours.

Removing the SiO2 layer after the oxidation using Vapored HF tool with recipe# 2 and time=5 minutes.

Result:

Figure 4. Reduced Si nanowire, through thermal oxidation and following vapored HF etch, profile. a) Cross-section view, b) 70 degree title view; c) another 70 degree title view d) one more 70 degree title view.





The averaged diameter of the nanowire is 61.0 nm.

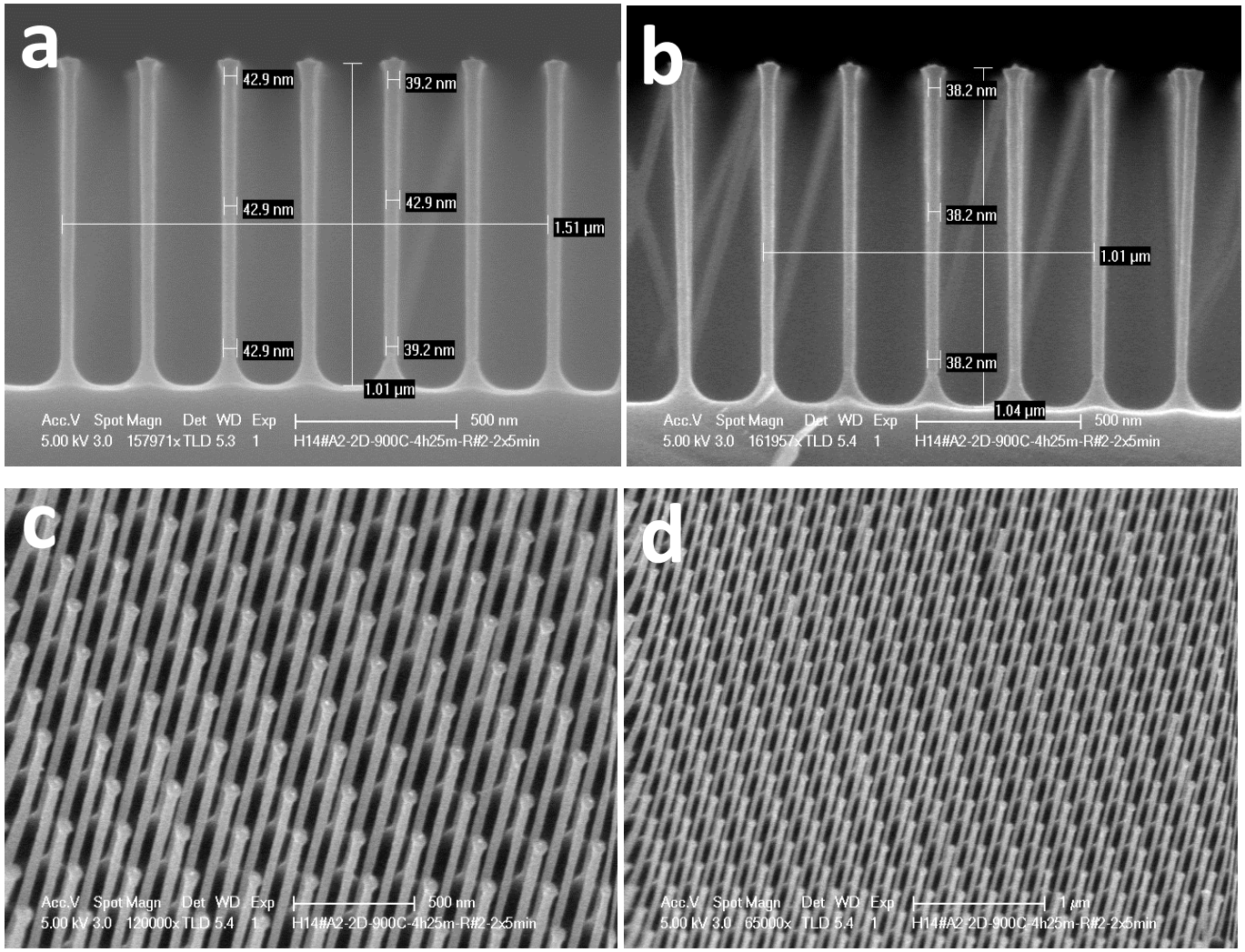
This indicates that, after the thermal oxidation and following vapored HF process, **the diameter of the nanowires is reduced by ~45.8 nm** (116.8-61.0)!

2) Test#2

The target SiO2 layer thickness=40 nm: Dry thermal oxidation was carried out at a temperature of 900 C and time of 4 hours 25 minutes. Removing the SiO2 layer after the oxidation using Vapored HF tool with recipe# 2 and time=10 minutes (5minx2).

Result:

Figure 5. Reduced Si nanowire, through thermal oxidation and following vapored HF etch, profile. a) Cross-section view, b) another cross-section view; c) 45 degree title view d) another 45 degree title view.



The averaged diameter of the nanowire is 42.3 nm.

This indicates that, after the thermal oxidation and following vapored HF process, **the diameter of the nanowires is reduced by ~64.5 nm** (116.8-42.3)!