UNIVERSITY OF CALIFORNIA SANTA BARBARA
ELECTRICAL AND COMPUTER ENGINEERING

Towards THz Transistors & Template Assisted Selective Epitaxy

InAs/InP MOS-HEMTs with f_τ > 480 GHz

Template Assisted Selective Epitaxy on InP & Si

Brian Markman

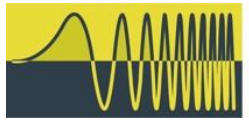
Nanofab Tech Talk

UCSB Department of Electrical and Computer Engineering

September 12th, 2019

JUMP
Joint University Microelectronics Program

Advisor: Prof. Mark Rodwell



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Funding: SRC, NSF, DARPA

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Brian Markman, University of California, Santa Barbara, CA

Abstract: As 5G (25-100GHz) begins to roll out globally, research must shift focus to communication systems beyond 5G (>100 GHz). For communications systems to work efficiently at 100-340 GHz, the transistors that form their foundation must be able to provide gain and low noise figure at those frequencies. Consequently, the transistors must operate beyond 1 THz. However, a highly scaled MOSFET's RF performance is limited by end capacitance while modern HEMTs are limited by high gate leakage and comparatively less capacitive control of the channel. We present a new device that combines an intrinsic MOSFET with HEMT-like access regions operating to and a roadmap to >1 THz. Additionally, template fabrication for template assisted selective epitaxy (TASE) will be discussed as a route towards higher frequency bipolar transistors, integration of III-V on Si, and as a technique to develop laterally oriented heterojunction devices. Challenges in template fabrication, basic growth trends, and design considerations will be discussed.

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1. **MOS-HEMT Introduction**
   - Beyond 5G Application
   - Design Challenges
   - Proposed InAs/InP MOS-HEMT Design
2. **THz Transistor "Pieces"**
   - Fabrication Process
   - High-k Quality
   - Modulation Doped Access Regions
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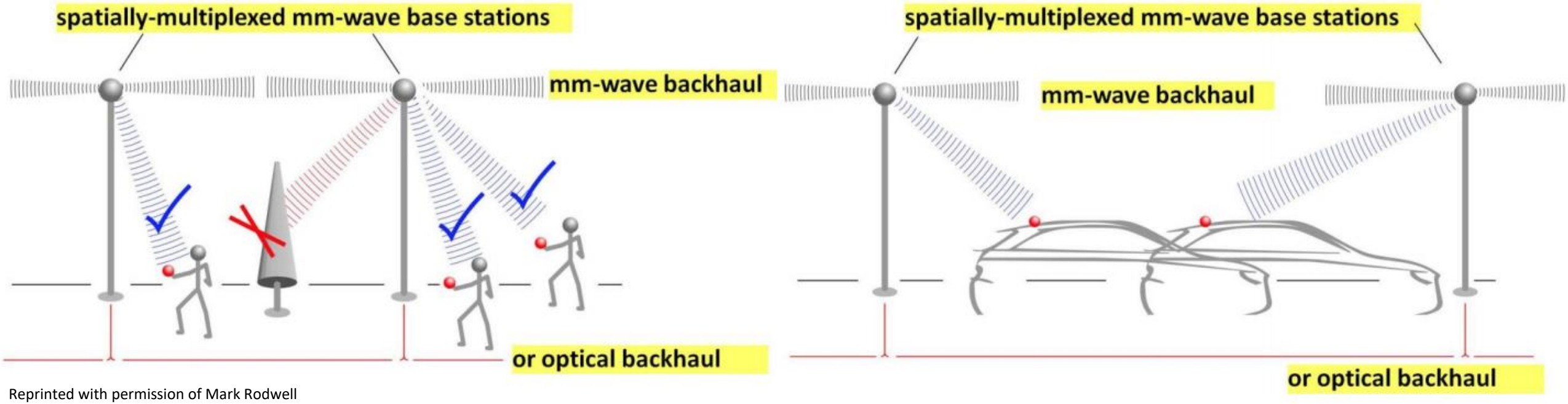
Motivation – Beyond 5G

- Demand for information/connectivity increasing explosively



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- Industry currently introducing 5G (28, 38, 57-71, 71-86 GHz)
- Beyond 5G requires 100-340 GHz communication systems
- Wireless for End-User and Backhaul will require higher data rates

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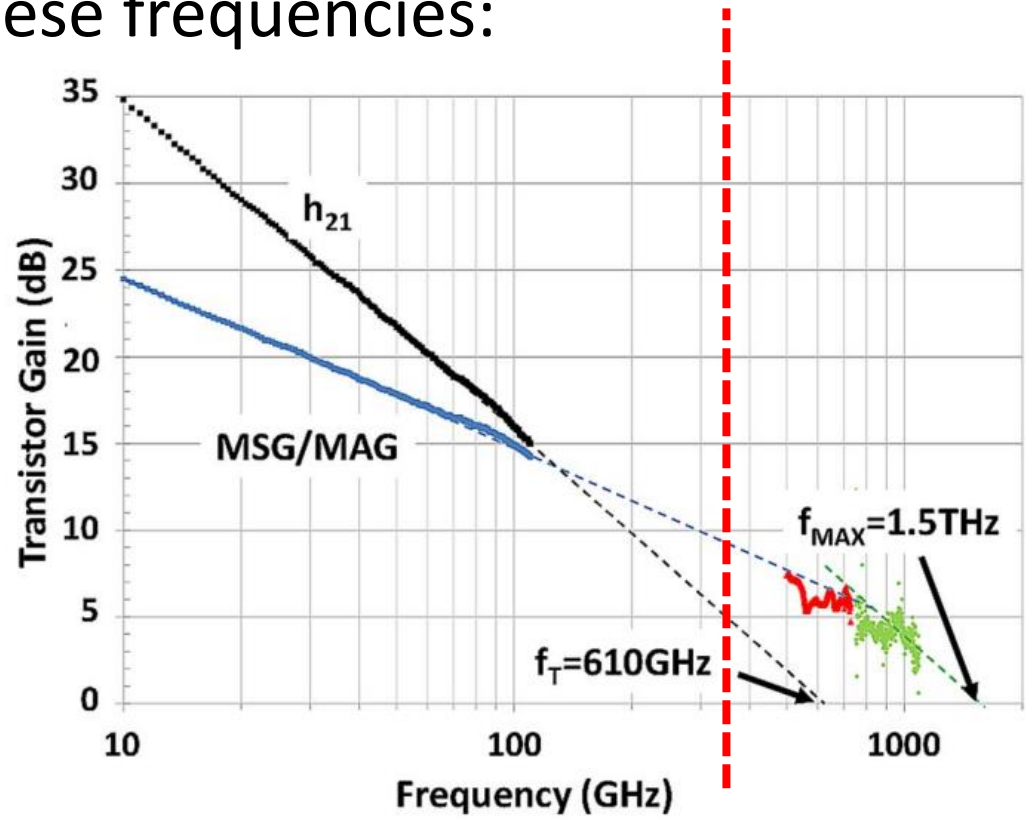
$$\sim \frac{1}{10} f_\tau, f_{max} \rightarrow \underline{\text{NEED GAIN}}$$

f_τ = current gain cutoff frequency

f_{max} = power gain cutoff frequency



X. Mei *et al.* IEEE EDL vol. 36, No. 4, 2015.

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How to increase f_τ?

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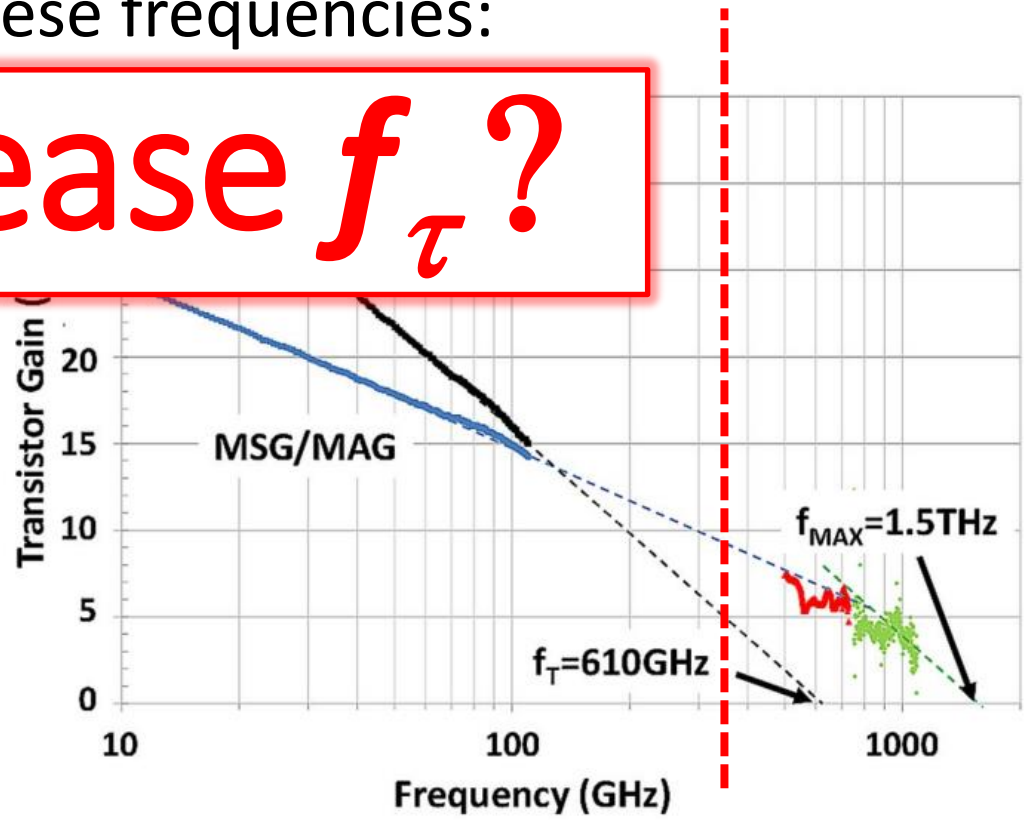

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Increase f_τ

- *Ideal: Transit Time*

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How to Increase $g_{m,i}$? Look to Ballistic FET Theory

- Electron travels S → D without scattering, can derive IV from E(k)
- High-k roughness/non-epitaxial interface, $L_g < 30nm$
- Independent of L_g → except short channel effects

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qn_s

Injection velocity

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Traditional FET Scaling Laws (Now Broken)

FET parameter	change
gate length	decrease 2:1
current density (mA/mm)	increase 2:1
specific transconductance (mS/mm)	increase 2:1
transport mass	constant
2DEG electron density	increase 2:1
gate-channel capacitance density	increase 2:1
dielectric equivalent thickness	decrease 2:1
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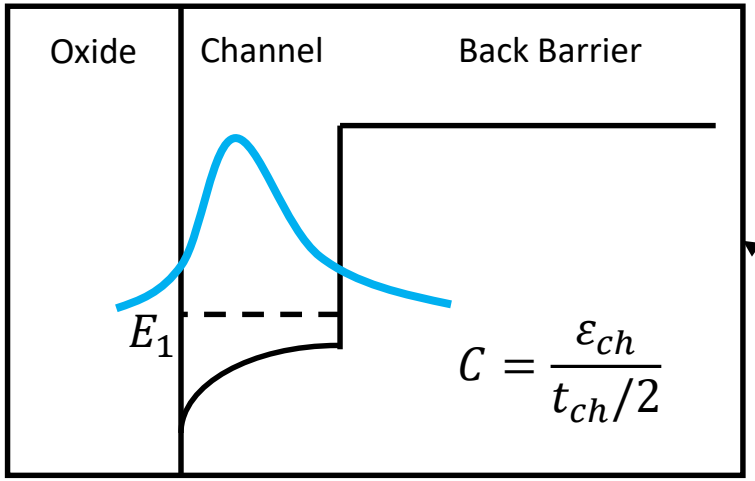
channel state density	increase 2:1
contact resistivities	decrease 4:1

FET Scaling Laws (Now Broken)

Wave function has "thickness"



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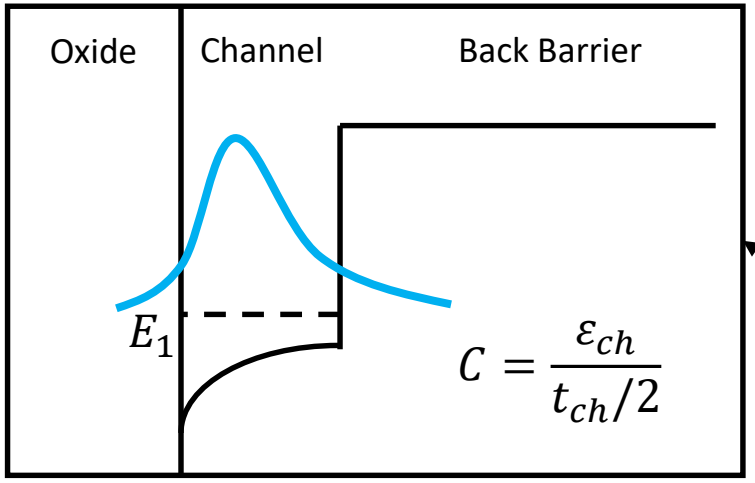
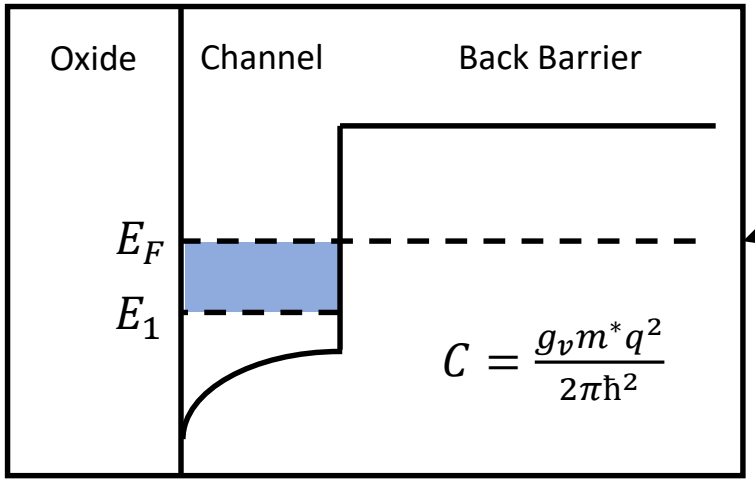


Fermi Level moves to populate low DOS



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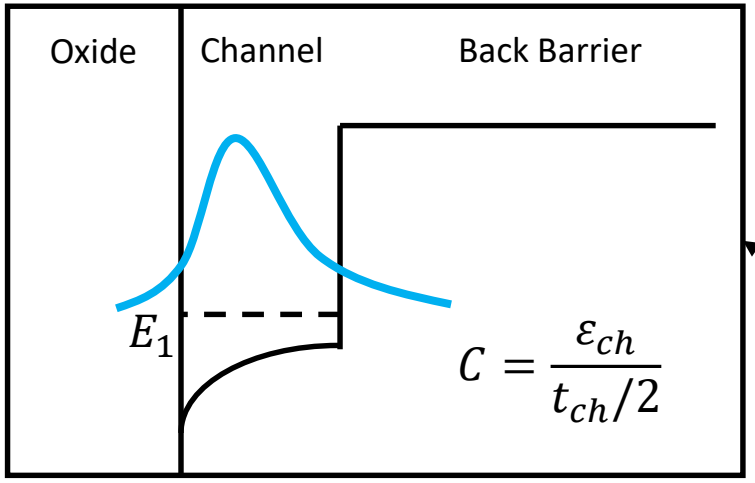

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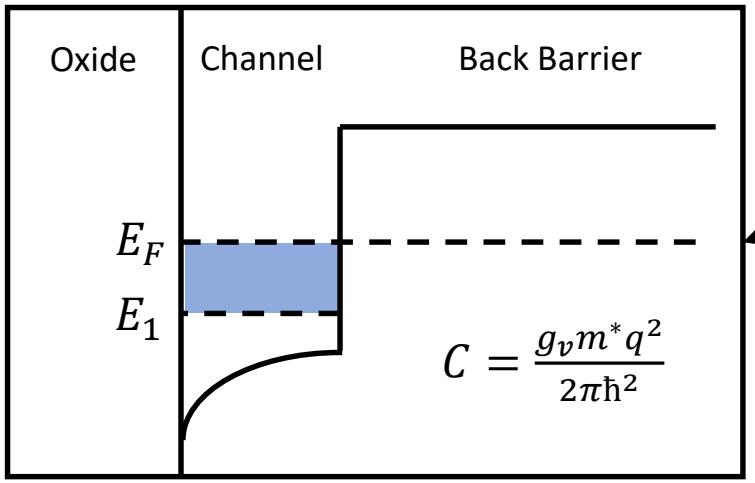

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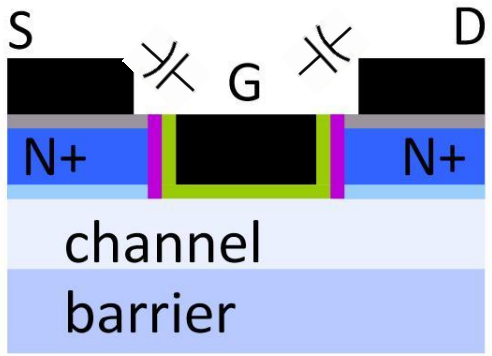

- vertical S/D spacer
- low-K dielectric spacer
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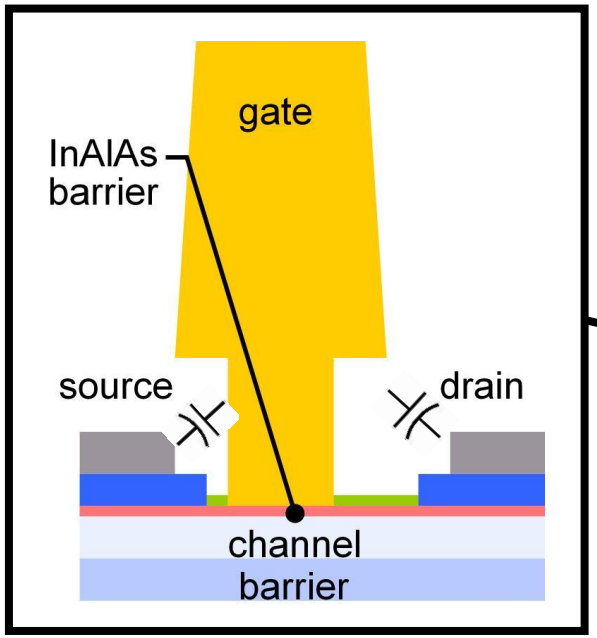
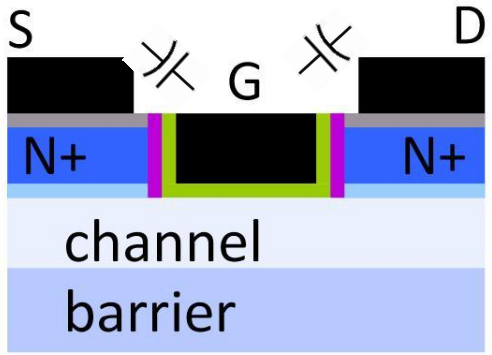
Highly scaled MOSFETs have large C_{end} due to packing density





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What about HEMTs ?

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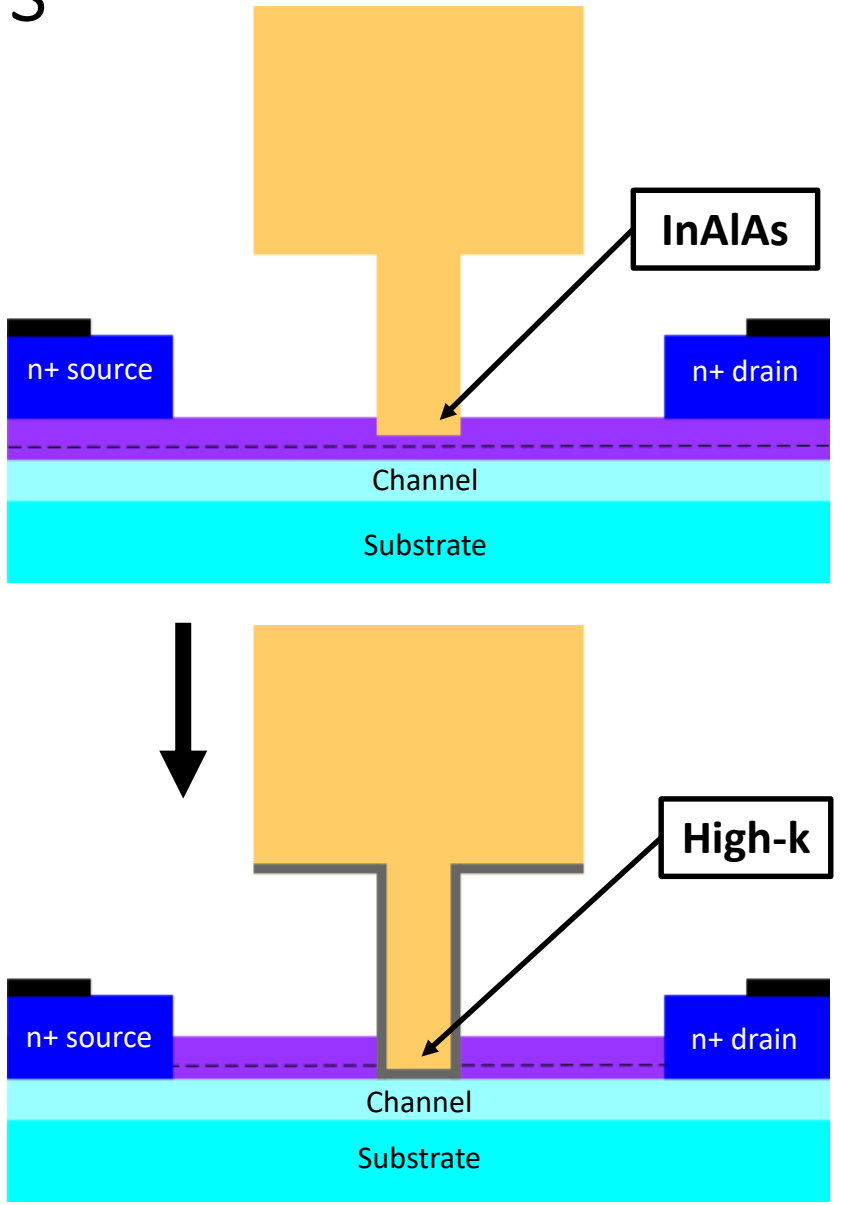
Towards faster HEMTs

Scaling limit: Gate Insulator Thickness

- **HEMT:** InAlAs barrier: tunneling, thermionic leakage
  - CBO ~ 0.5eV to InGaAs
- **Solution:** replace InAlAs with high-K dielectric
  - CBO > 3.0eV to InGaAs
- **Target:** 2nm ZrO_2 (ε_r=25) vs. 5nm InAlAs (ε_r=12) : adequately low leakage
  - 70% improvement of C_{g-ch}



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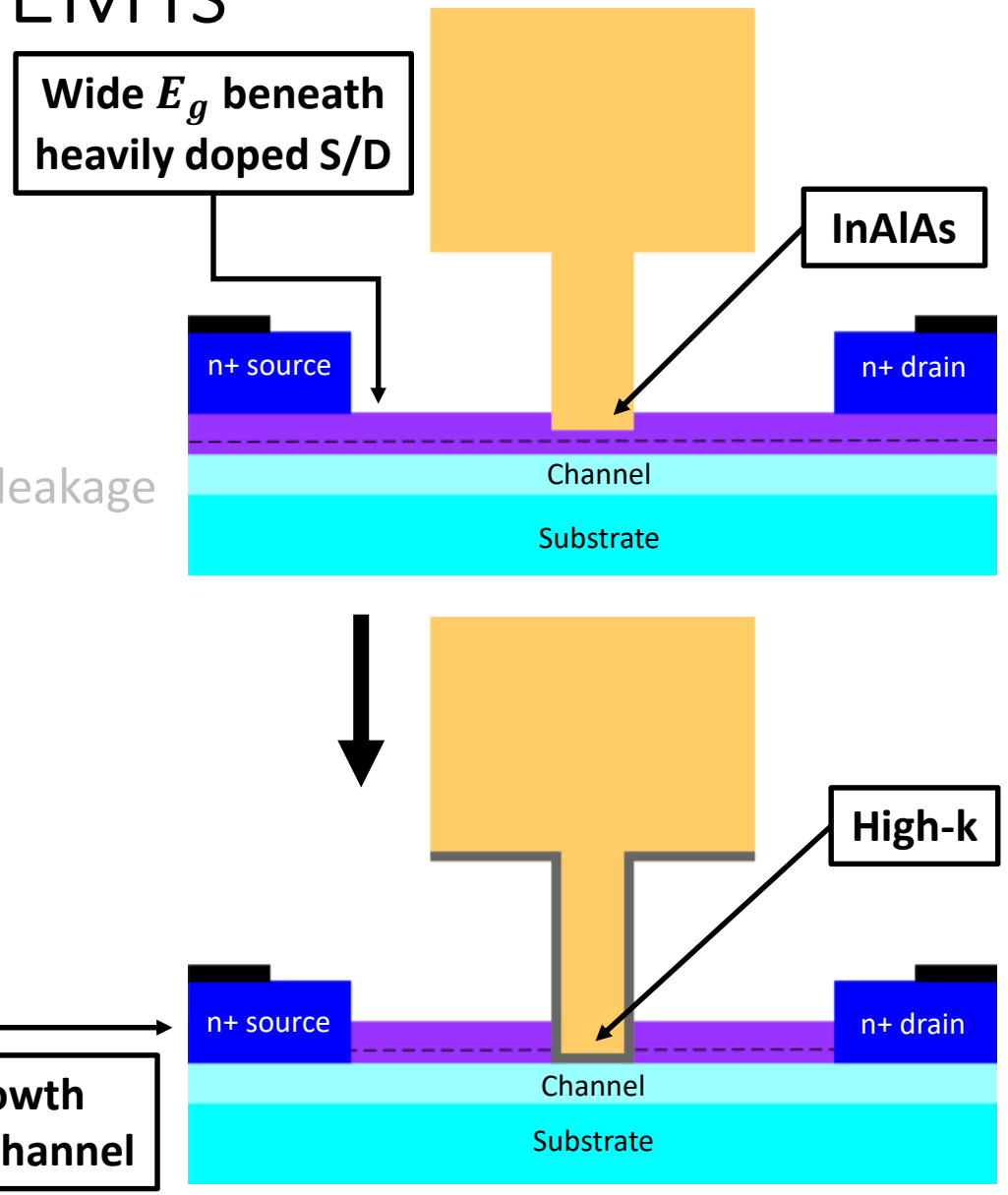
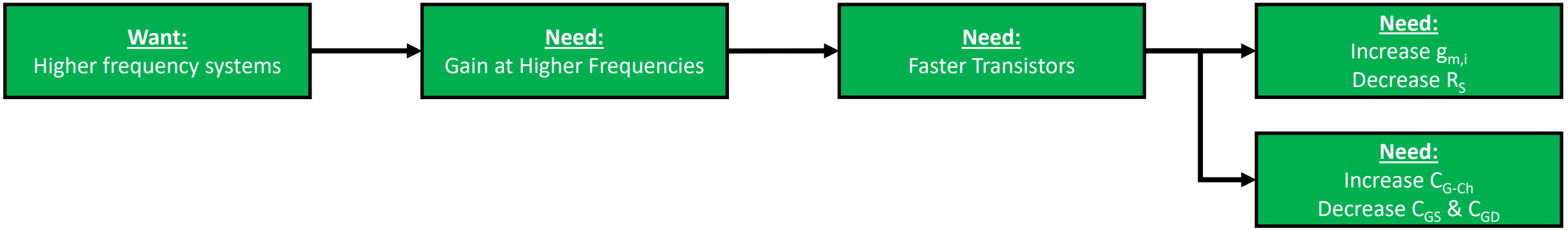
Scaling limit: Wide E_g beneath S/D

- **HEMT:** InAlAs barrier is **under** N+ source/drain
  - $\sim 100\ \Omega \cdot \mu m$ in R_S
- **Solution:** regrowth, place N+ layer on InAs channel
  - No barrier between S/D and channel
- **Target:** Removes $100\ \Omega \cdot \mu m$ from $g_{m,e} = 3\ mS/\mu m$
  - ~30% improvement in $g_{m,e}$



Summary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Summary

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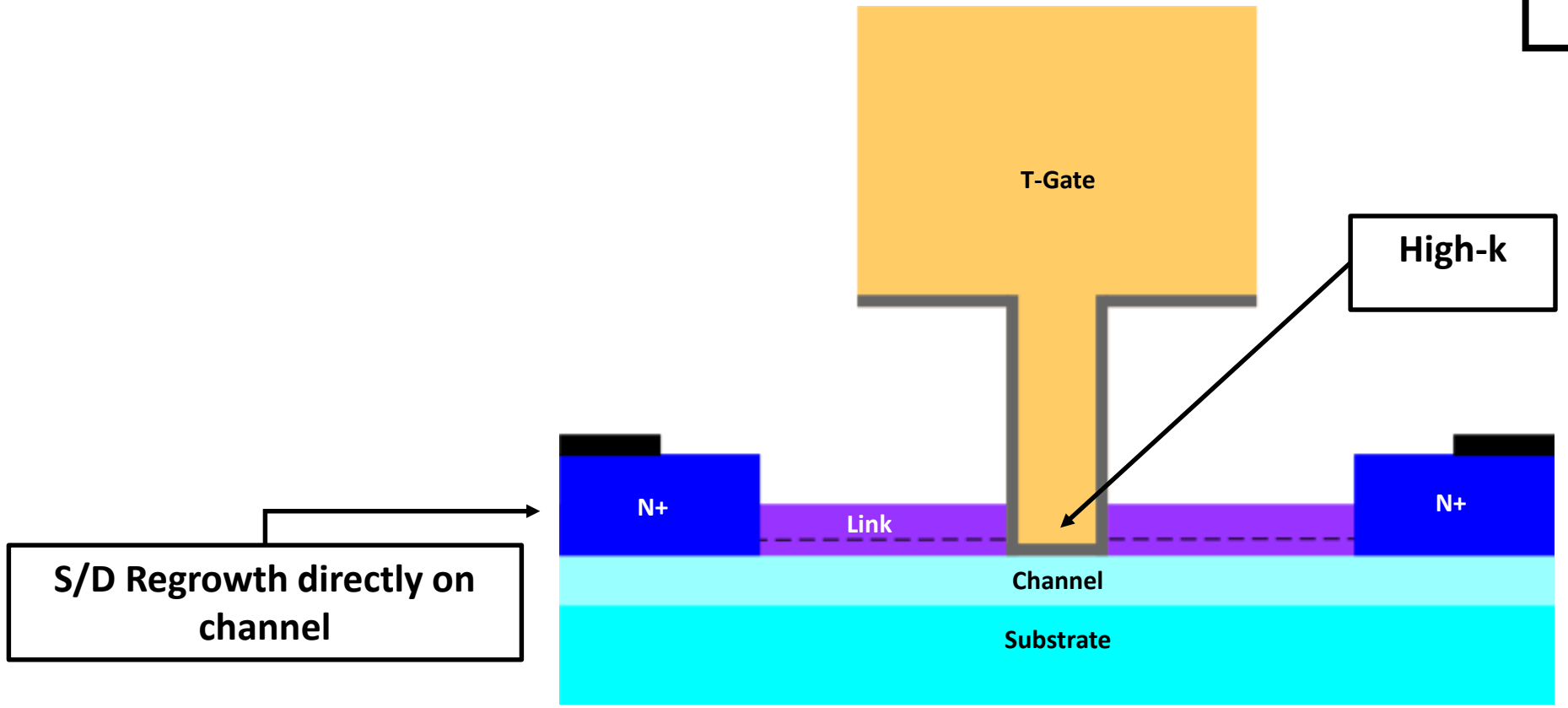

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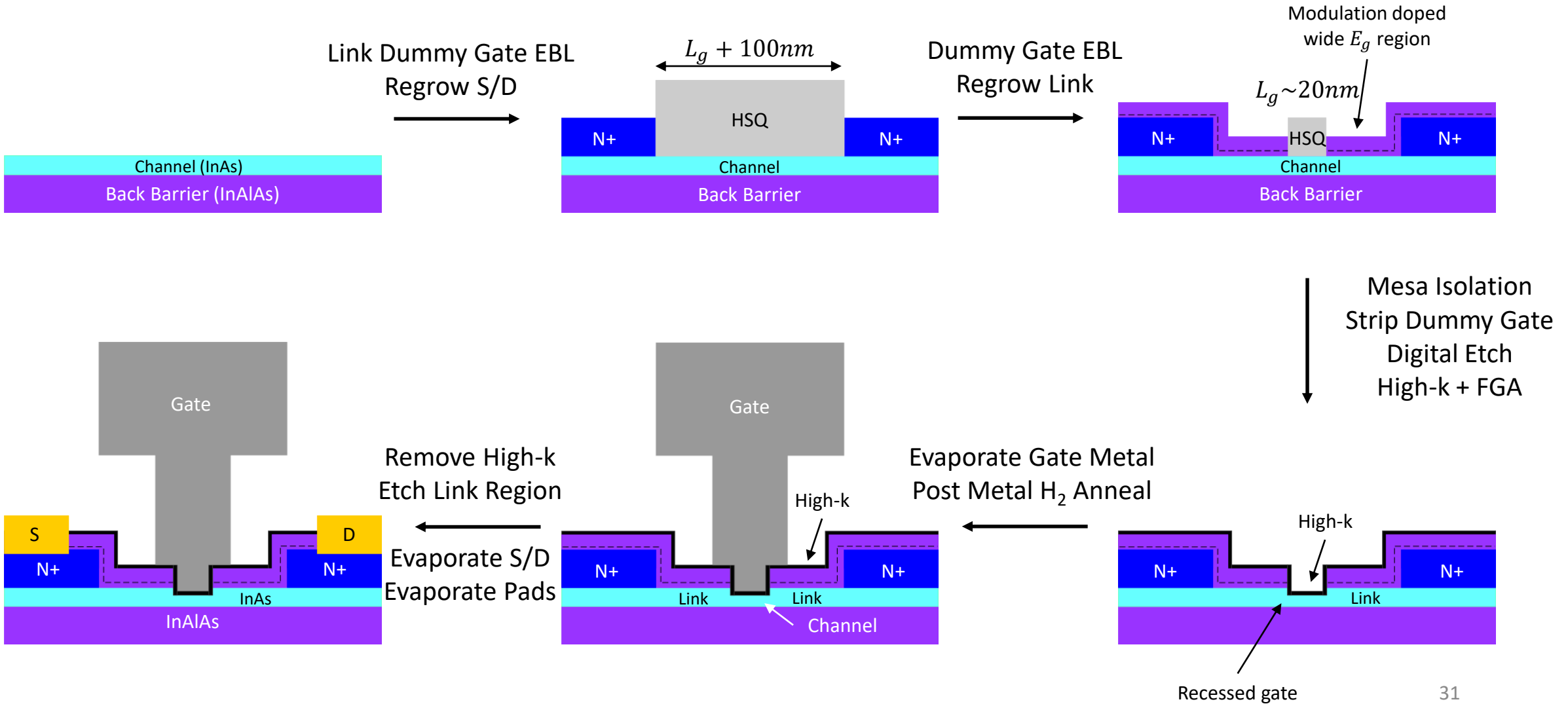
Regrowth Reversal Process



Need Pieces First

Major Components:

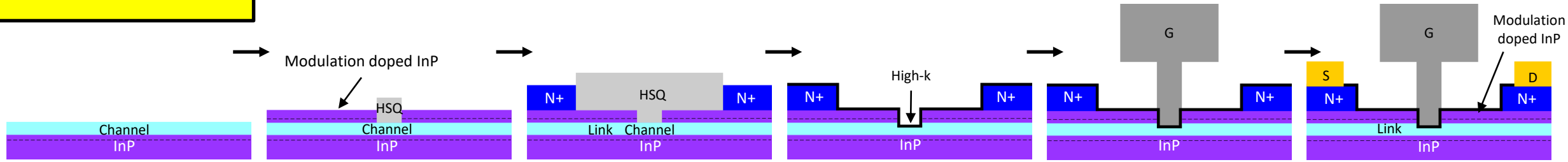
1. High quality gate oxide (ZrO_2)
   a) Varistha Chopattana. PhD Dissertation, UCSB, 2016.
   b) Sanghoon Lee. PhD Dissertation, UCSB, 2014.
   c) Cheng-Ying Huang. PhD Dissertation, UCSB, 2015.
   d) Hsin-Ying Tseng *et al.* DRC, paper 2019.
2. Modulation doped access region
   a) H.B. Jo *et al.* Appl. Phys. Express vol. 12, 2019.
   b) Simoné Growth / Klamkin Group InP MOCVD
3. RF Process All Together
   a) J. Wu *et al.* IEEE EDL vol. 39, No. 4, 2018.

9 cycles TMA + N* \ 100W – 300C
~35 cycles TEMAZ + H_2O – 300C

Channel Material	Minimum SS
InAs [1a,1b]	61 mV/dec
InGaAs [1c]	63 mV/dec
InP / InGaAs [1c]	67 mV/dec
InP [1d]	71 mV/dec

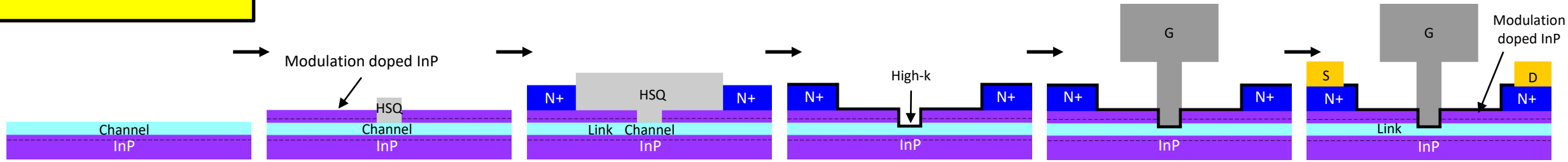
RF MOSFET

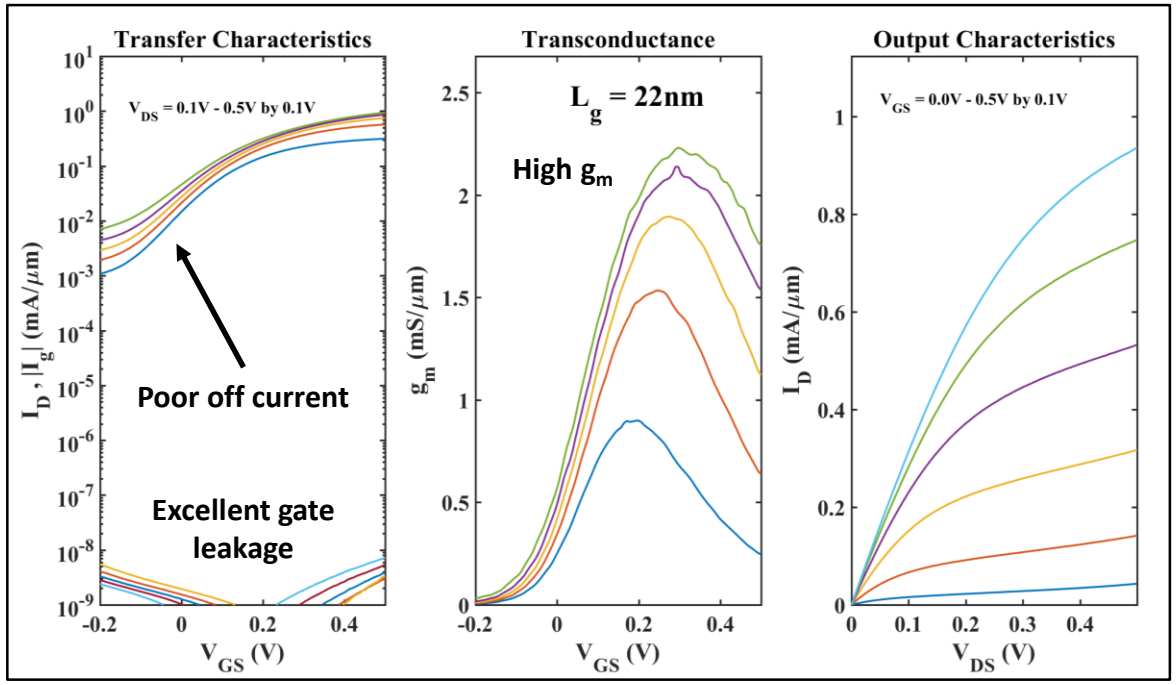
RF MOSFET DC Results – Ch3-L1G2SD3

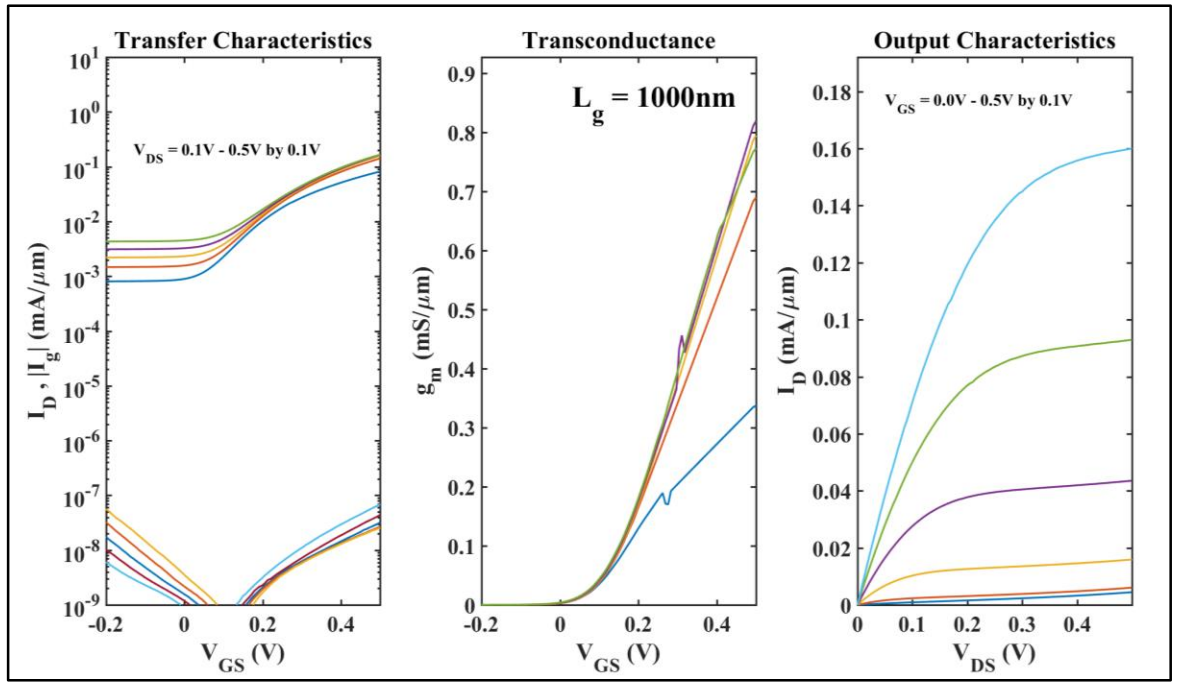


RF MOSFET

RF MOSFET DC Results – Ch3-L1G2SD3



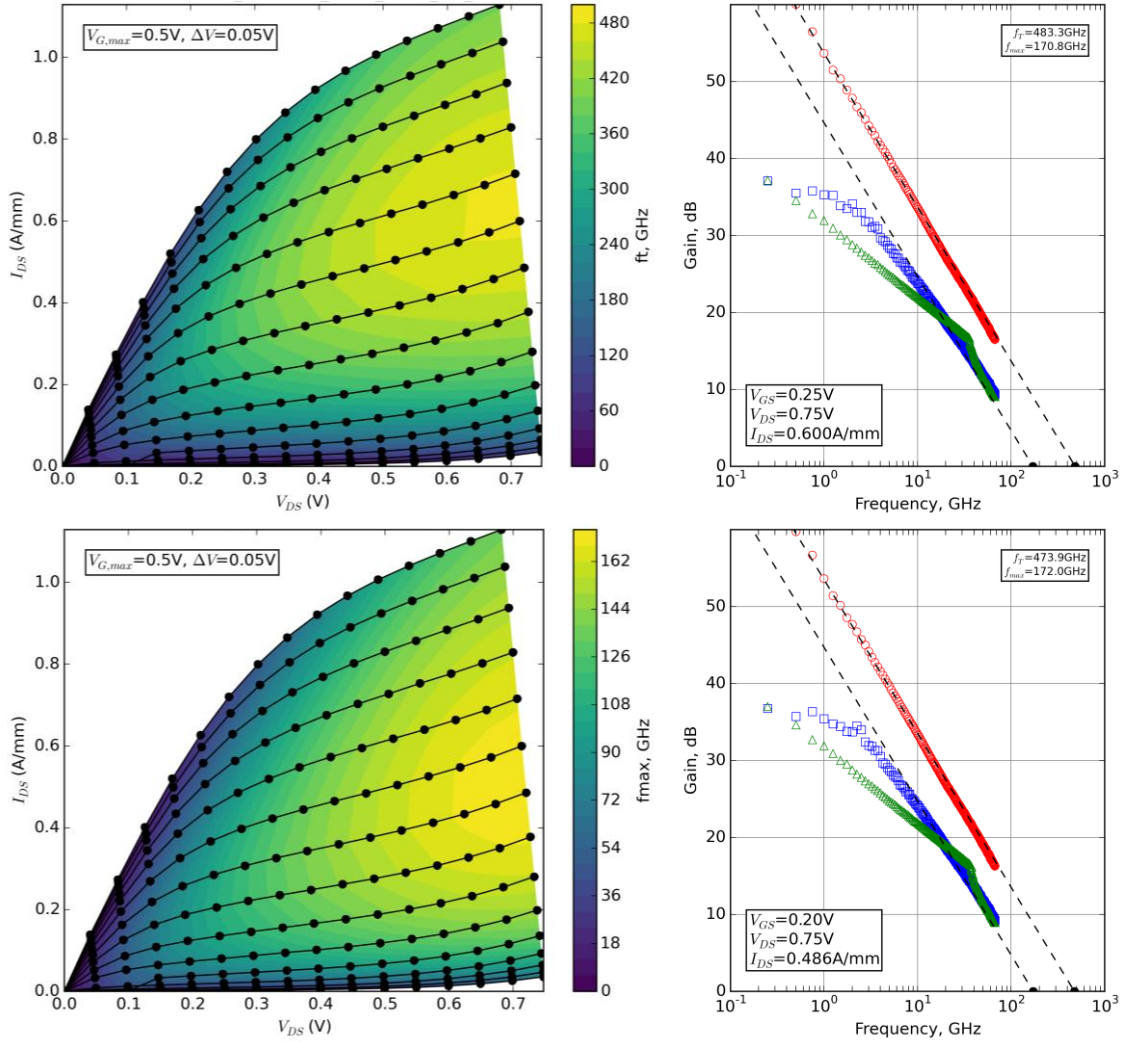




- Pinch off and SS mostly convoluted with S/D leakage → parallel conduction in etch stop
- Excellent gate leakage (I_g < 10 pA/μm for T-Gate devices, L_{foot} < 200nm)
- Ion ~ 1 mA/μm and peak $g_{m,e}$ = 2.3 mS/μm → **EXCELLENT** given thick channel & high-k

RF MOSFET

L_g = 22nm, W_g = 20µm RF Results – Ch3-L1G2SD3



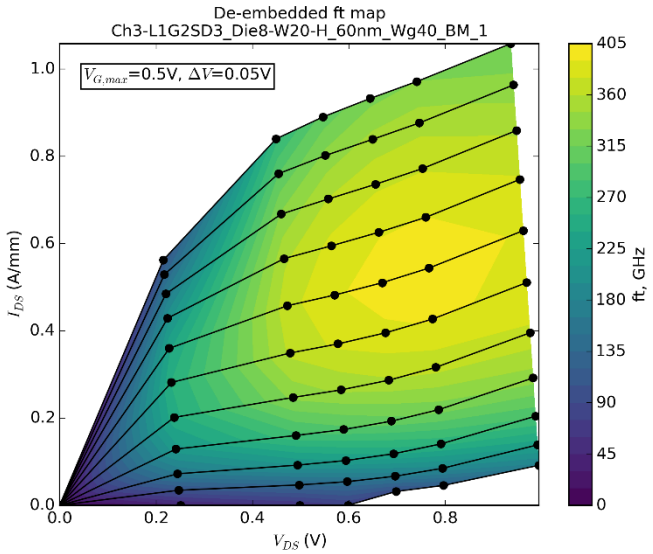
RF measurements & graphs courtesy of Matt Guidry

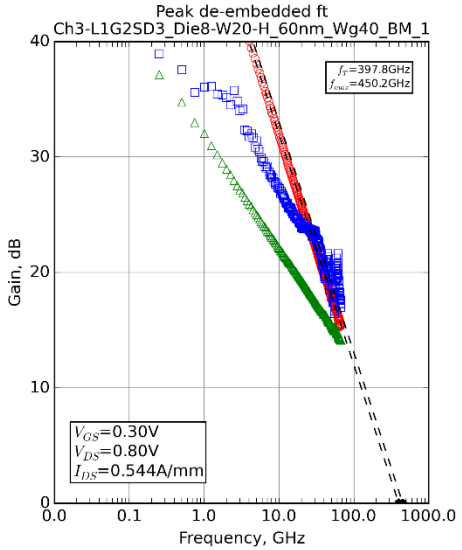
	Ch3-L1G2SD3
L_g	22 nm
W_g	40 µm
$g_{m,e}$(DC)	2.33 mS/µm
$g_{m,e}$(1 GHz)	2.65 mS/µm
f_t	**480 GHz**
f_{max}	**170 GHz**

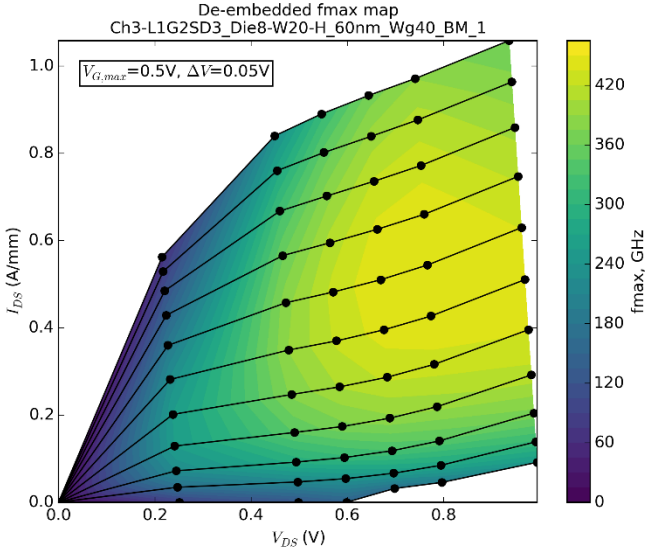
Poor f_{max} due to gate resistance → T-Gate Necking

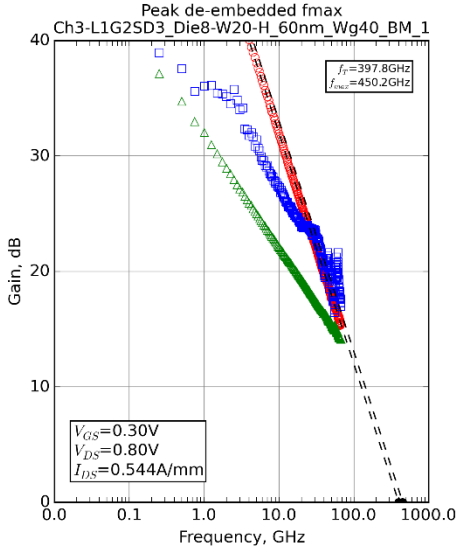
RF MOSFET

Ch3-L1G2SD3 – Device Comparison









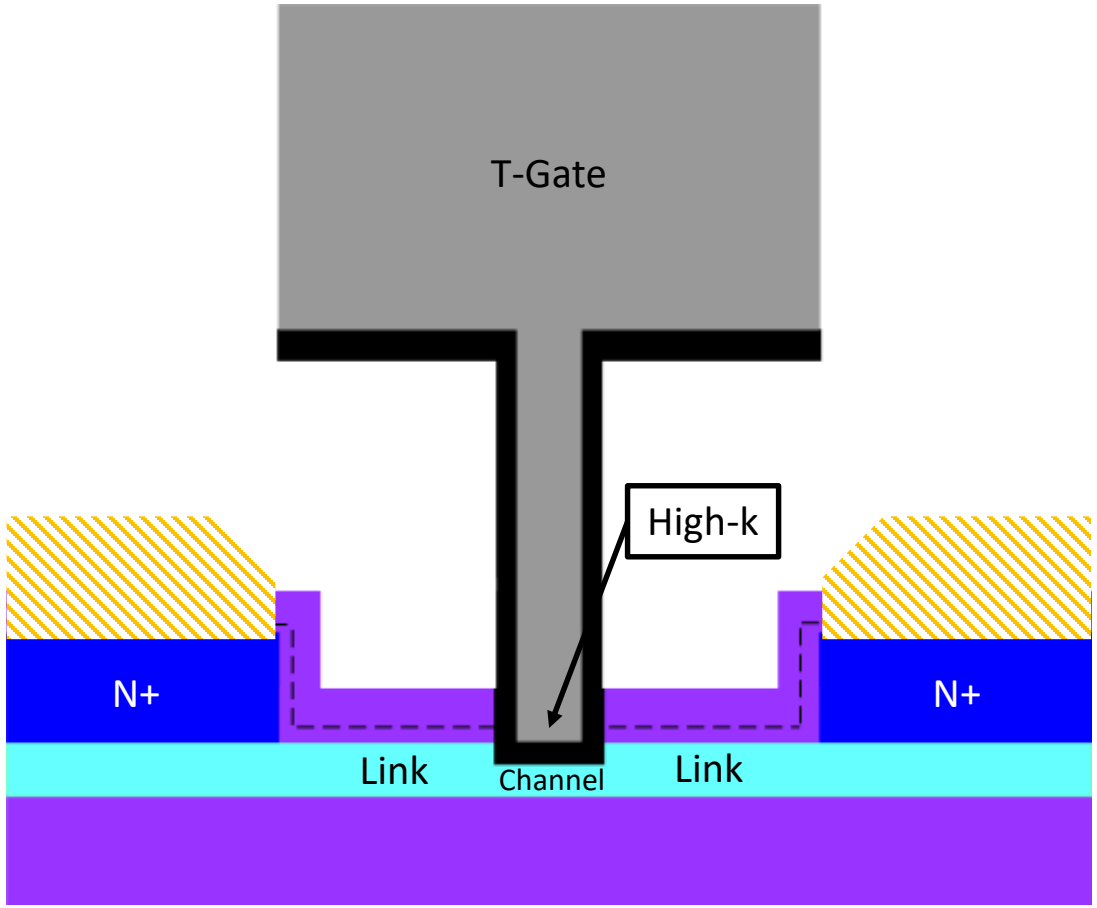
	22nm	60nm
L_{foot}	74 nm	100nm
W_g	40 µm	40 µm
f_t	**482 GHz**	**397 GHz**
f_{max}	**202 GHz**	**450 GHz**

- Do not pay attention to actual numbers → poor calibration ISS and bad probes
- Gate resistance is limiting factor on this run

RF measurements & graphs courtesy of Matt Guidry

What we are working on…

Parameter	Quantity
$g_{m,i}$ (t_{ch} = 4nm)	4 mS/μm
R_C	10 Ω•μm
R_N	10 Ω•μm
R_L	10 Ω•μm
R_A	0 Ω•μm
$g_{m,e}$	3.57 mS/μm
C_{OX} (t_{OX} = 2nm, t_{int} = 1nm)	1.34 fF/μm
C_{DOS}	0.80 fF/μm
C_{QW}	1.63 fF/μm
$C_{GS,Fringe}$ (from NTT)	0.40 fF/μm
$C_{GD,Fringe}$ (from NTT)	0.10 fF/μm
f_t	896 GHz
f_{max}	1045 GHz

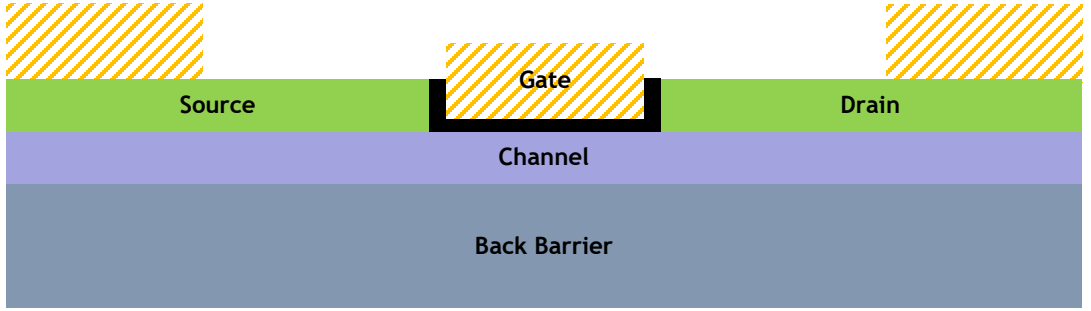


1. **MOS-HEMT Introduction**
   - Beyond 5G Application
   - Design Challenges
   - Proposed InAs/InP MOS-HEMT Design
2. **THz Transistor "Pieces"**
   - Fabrication Process
   - High-k Quality
   - Modulation Doped Access Regions
   - $f_\tau = 480\ GHz$ MOS-HEMT demonstration
3. **Template Assisted Selective Epitaxy (TASE) Introduction**
   - Heterogenous Integration & Heterojunction Turning
   - Design Challenges & Fabrication Process
4. **TASE Examples**
   - Homo-epitaxy
   - Hetero-epitaxy
5. **Conclusions**

What is TASE?

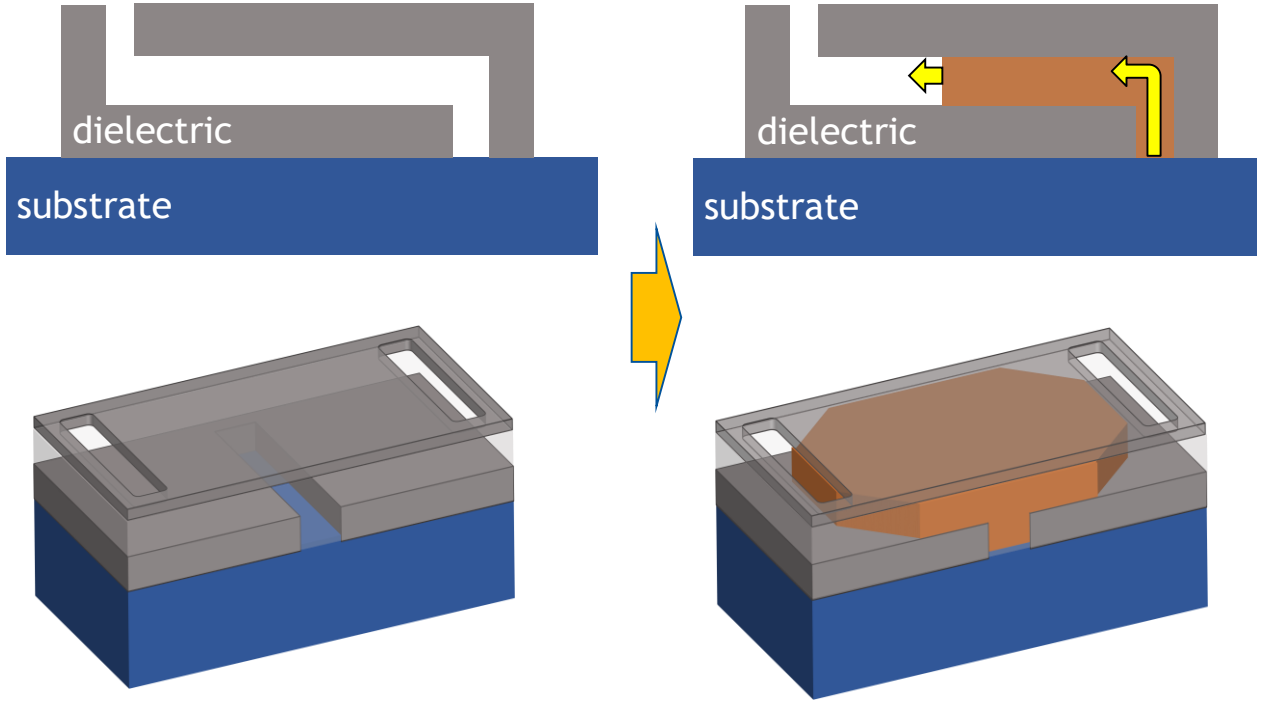
Standard approach:

Devices generally fabricated beginning with planar epitaxial layers

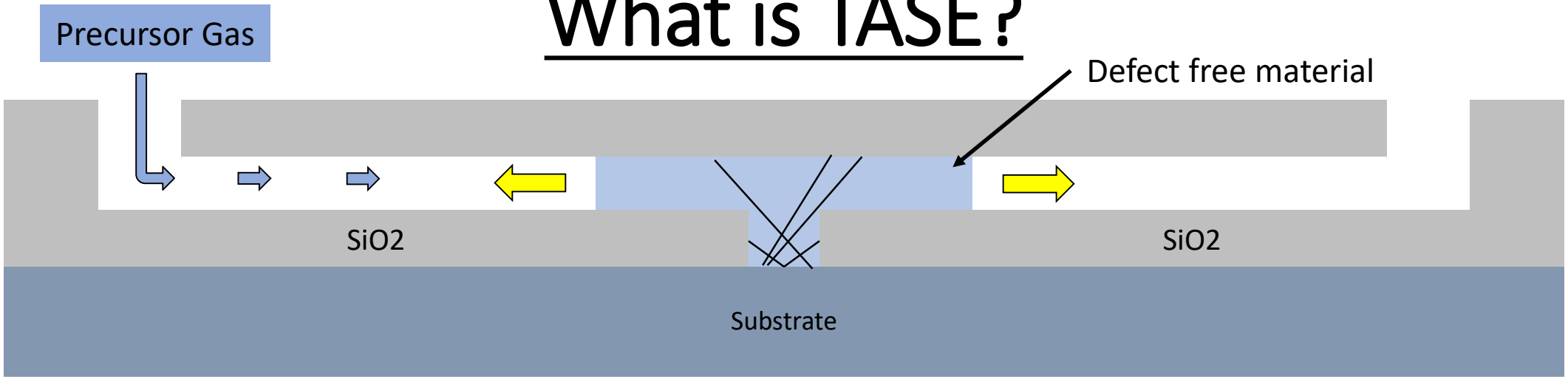


New approach:
Template Assisted Selective Epitaxy

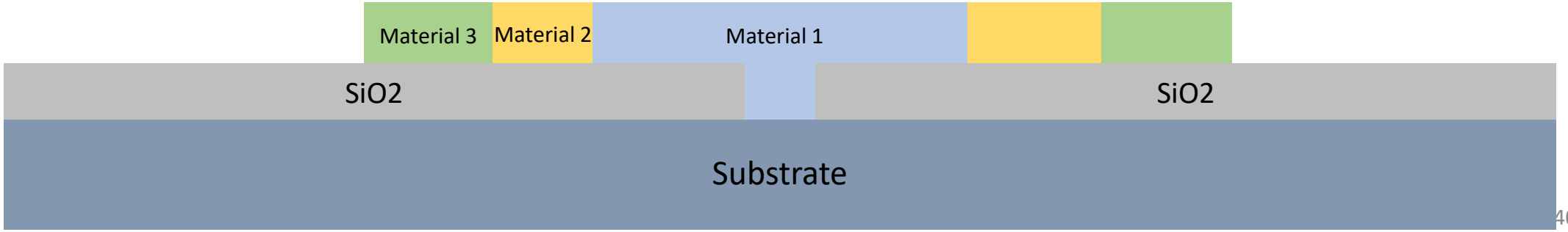
- Orientation and thickness defined by template
- Selective growth occurs laterally
- Confined in template of dielectric material



What is TASE?

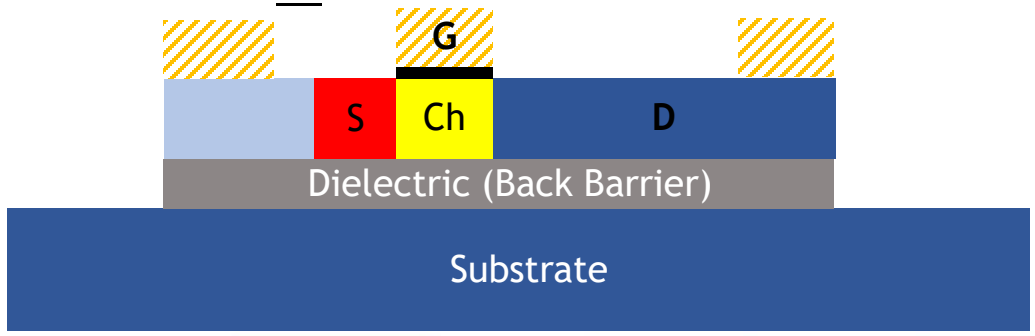


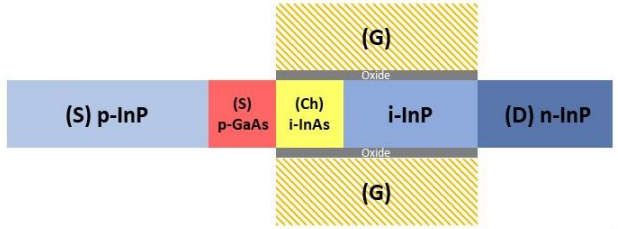
- Growth via MOCVD selectively initiates at the substrate and proceeds laterally
- Gives in-plane heterojunctions
- Can trap defects with box edges enabling monolithic integration



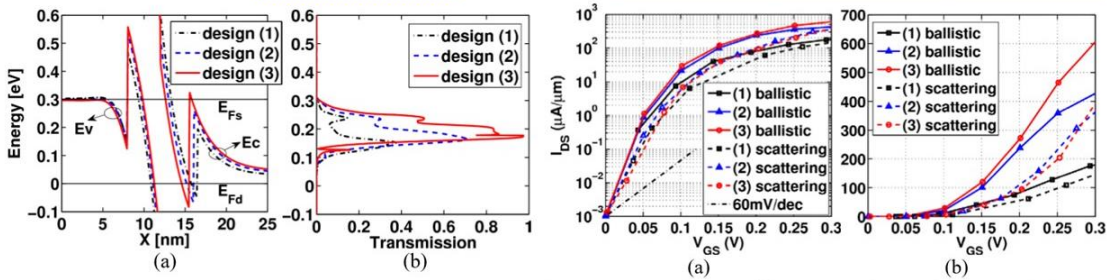
Why is it useful?

High I_{on} Triple HJ Tunnel FET





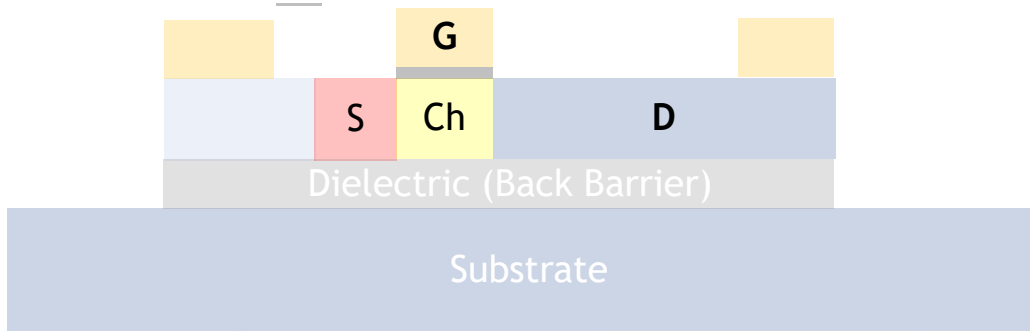
Design	Source Well	Channel Well
(1) Lattice Matched	$p-In_{0.53}Ga_{0.47}As$	$i-In_{0.53}Ga_{0.47}As$
(2) Lightly Strained	$p-In_{0.26}Ga_{0.74}As$ (1.91% tensile)	$i-In_{0.77}Ga_{0.23}As$ (1.62% compressive)
(3) Heavily Strained	$p-GaAs$ (3.81% tensile)	$i-InAs$ (3.13% compressive)

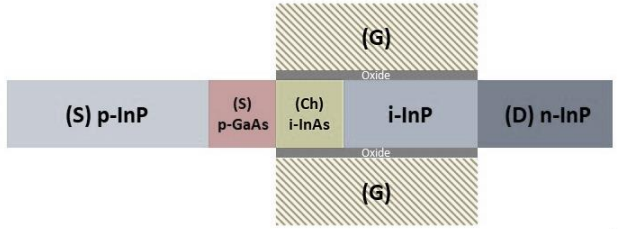


- Simple post-growth process flow
- Lateral gating and VLSI compatible processing
- Channel thickness controlled by template

Why is it useful?

High I_{on} Triple HJ Tunnel FET





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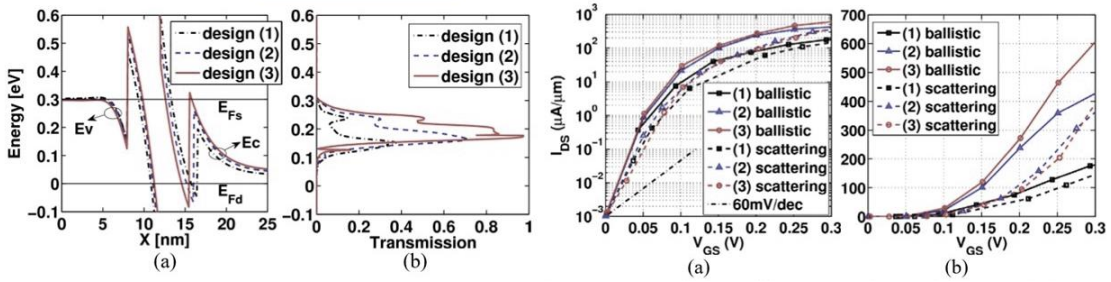

- Simple post-growth process flow
- Lateral gating and VLSI compatible processing
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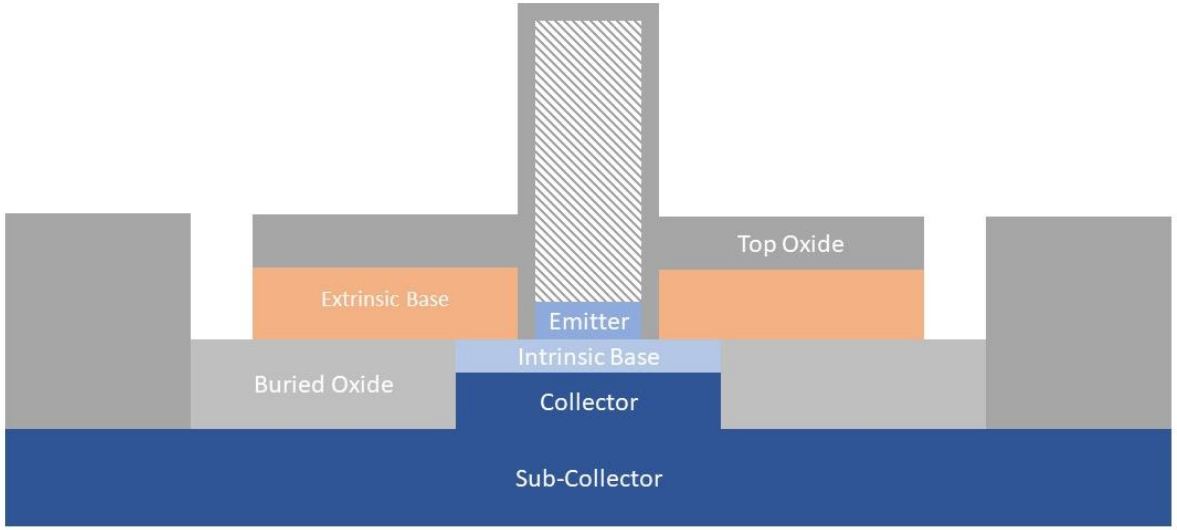
Regrown Extrinsic Base HBT



$$f_{max} \cong \sqrt{f_\tau / 8\pi R_{bb} C_{cbi}}$$

- Simultaneous optimization of intrinsic device materials and extrinsic device materials
- Enables reduction in R_{bb} (optimize contacts)
- Simultaneous reduction in C_{cb} (buried oxide)

Why is it useful?

Heterogenous Integration: III/V on Si (IBM Zurich)

Confined Epitaxial Lateral Overgrowth (CELO): A Novel Concept for Scalable Integration of CMOS-compatible InGaAs-on-insulator MOSFETs on Large-Area Si Substrates

L. Czornomaz, E. Uccelli, M. Sousa, V. Deshpande, V. Djara, D. Caimi, M. D. Rossell*, R. Erni* and J. Fompeyrine
IBM Research GmbH Zürich Laboratory, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland
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Published Online: June 1998 Accepted: September 1989

Novel technique for Si epitaxial lateral overgrowth: Tunnel epitaxy

Appl. Phys. Lett. **55**, 2205 (1989); https://doi.org/10.1063/1.102061

Atsushi Ogura *and* Yuki Fujimoto

IEEE ELECTRON DEVICE LETTERS, VOL. 11, NO. 5, MAY 1990

Confined Lateral Selective Epitaxial Growth of Silicon for Device Fabrication

PETER J. SCHUBERT, STUDENT MEMBER, IEEE, AND GEROLD W. NEUDECK, FELLOW, IEEE

Nanotechnology **24** (2013) 225304 (6pp) doi:10.1088/0957-4484/24/22/225304

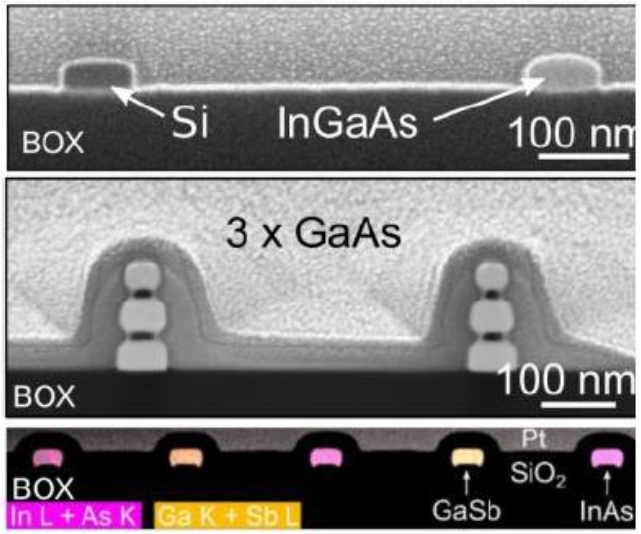
Selective area growth of III–V nanowires and their heterostructures on silicon in a nanotube template: towards monolithic integration of nano-devices

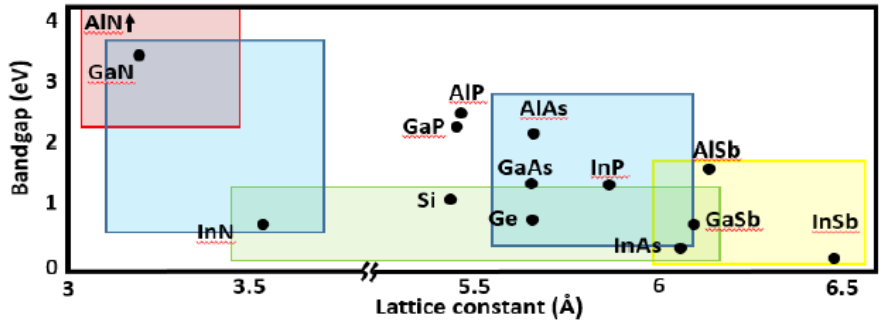
Pratyush Das Kanungo[1], Heinz Schmid[1], Mikael T Björk[2], Lynne M Gignac[3], Chris Breslin[3], John Bruley[3], Cedric D Bessire[1] and Heike Riel[1]

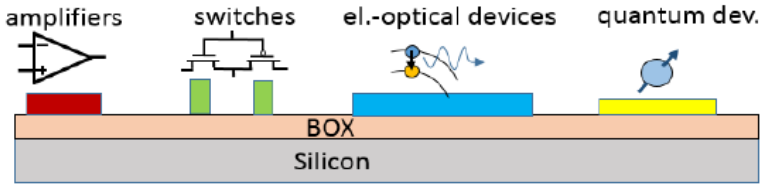
[1] IBM Research—Zurich, Säumerstrasse 4, 8803 Rüschlikon, Switzerland
[2] QuNano AB, Scheelevagen 17, Ideon Science Park, SE-22370 Lund, Sweden
[3] IBM Research—Watson, Yorktown Heights, NY 10598, USA

Monolithic integration of multiple III-V semiconductors on Si for MOSFETs and TFETs

H. Schmid, D. Cutaia, J. Gooth, S. Wirths, N. Bologna*, K. E. Moselund and H. Riel
IBM Research - Zurich, Säumerstrasse 4, 8803 Rüschlikon, Switzerland, email: sih@zurich.ibm.com
*EMPA, Electron Microscopy Center, 8600 Dübendorf, Switzerland

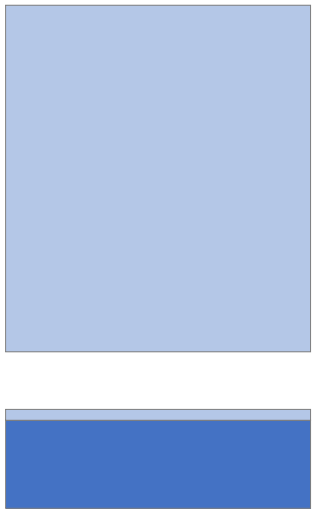




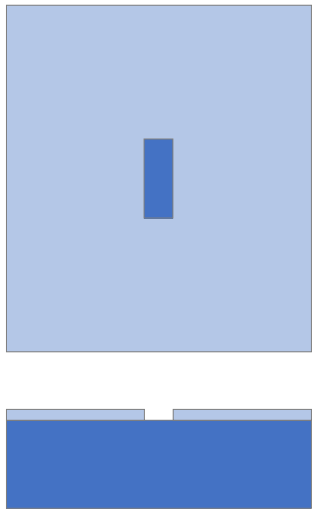


- Can integrate multiple material systems on single wafer
- Demonstration of MOSFETs and gain material promising

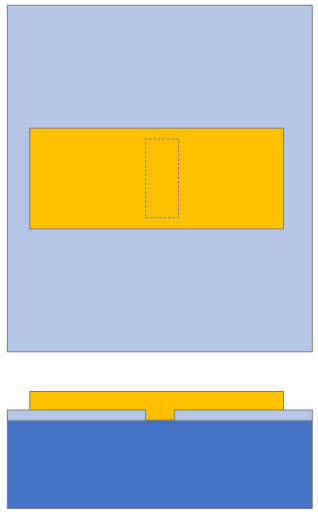
Fabrication Process



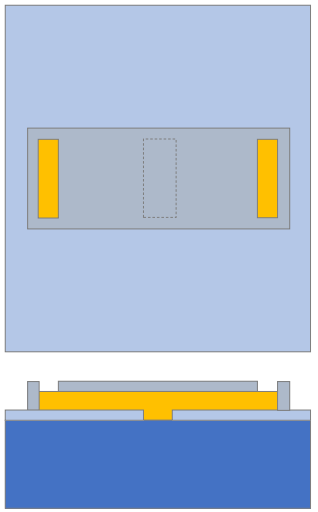
Bottom Oxide Deposition (PECVD)



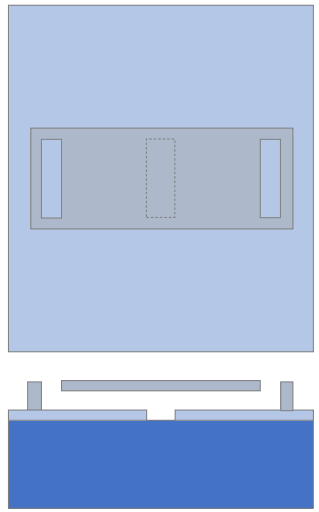
Seed Litho + Etch (EBL + ICP)



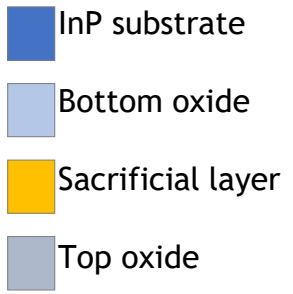
Sacrificial Layer Deposition + Litho + Etch (Sputter + EBL + ICP)

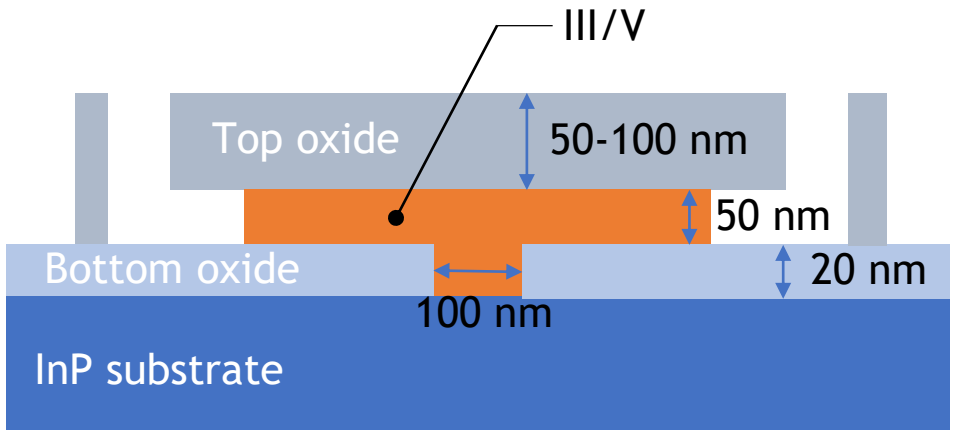


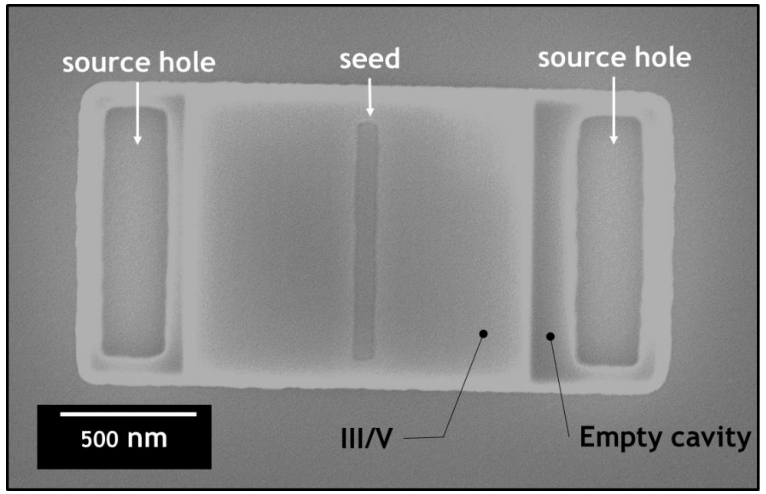
Top Oxide Deposition + Litho + Etch (PECVD + EBL + ICP)



Sacrificial Layer Removal (XeF2)





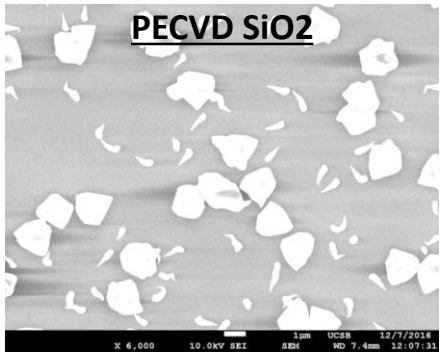


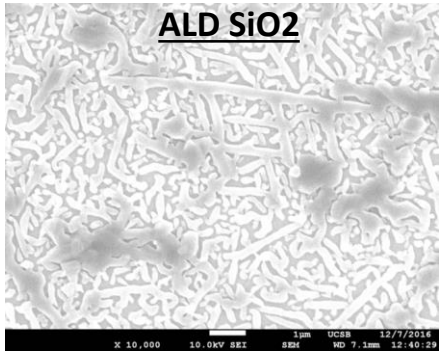
Design Considerations (III-V)

Design Considerations (III-V)

1. Growth Selectivity

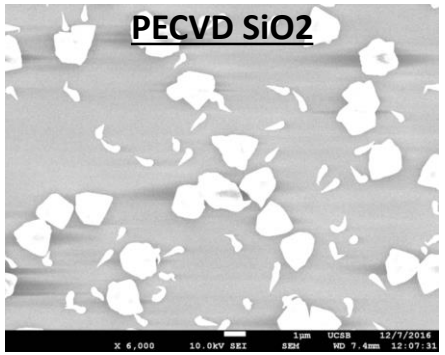
- Not all oxides are created equal, chose wisely

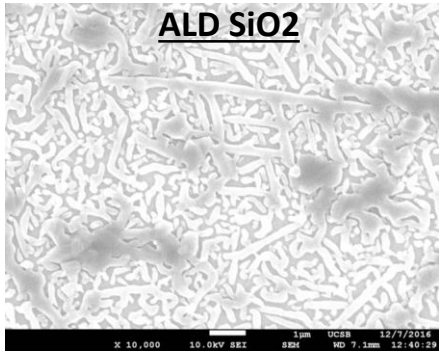


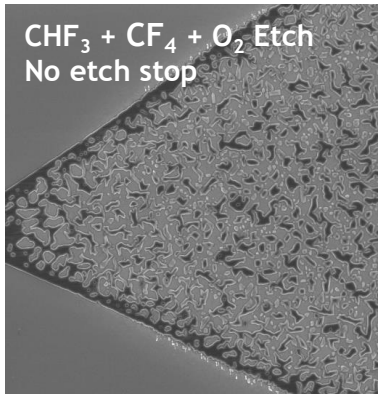


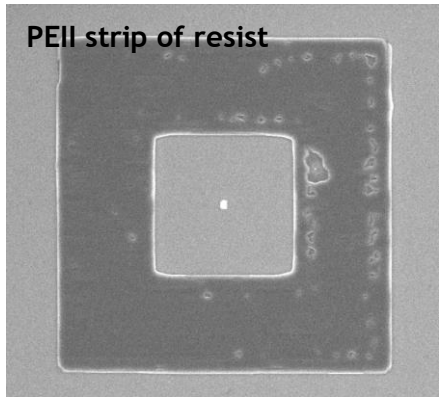
Design Considerations (III-V)

1. Growth Selectivity
   - Not all oxides are created equal, chose wisely
2. **Growth Window Definition**
   - Exposing surfaces to ion damage is bad for growth
   - May need very small opening → dry etch → etch stop, careful while stripping



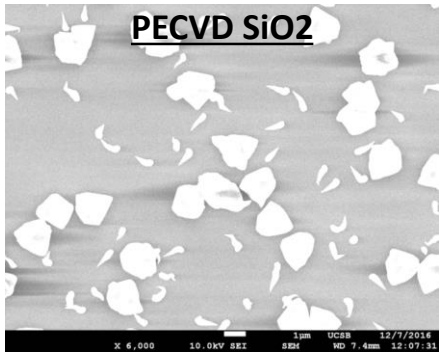


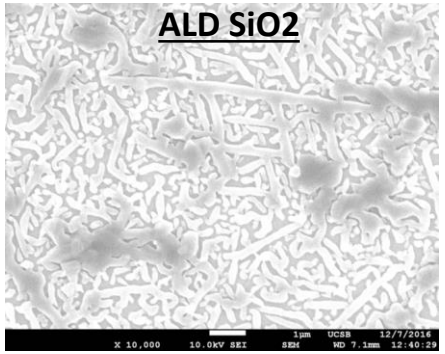




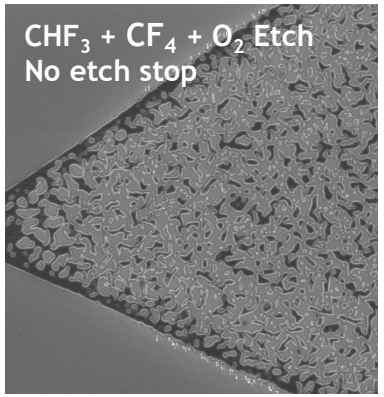
Design Considerations (III-V)

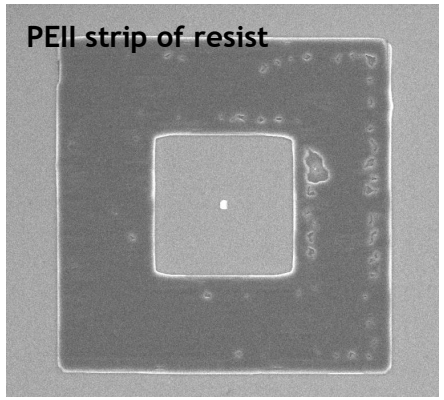
1. Growth Selectivity
   - Not all oxides are created equal, chose wisely
2. Growth Window Definition
   - Exposing surfaces to ion damage is bad for growth
   - May need very small opening → dry etch → etch stop, careful while stripping





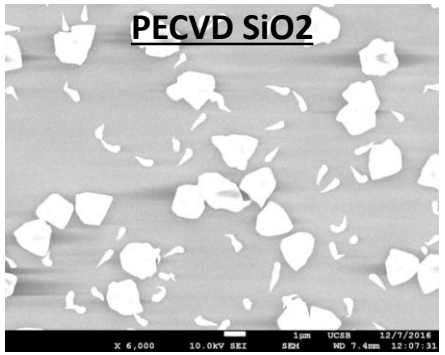
3. **Sacrificial Layer**
   - Defines cavity geometry/edges
   - Must be easily/selectively removed (resist or Si)

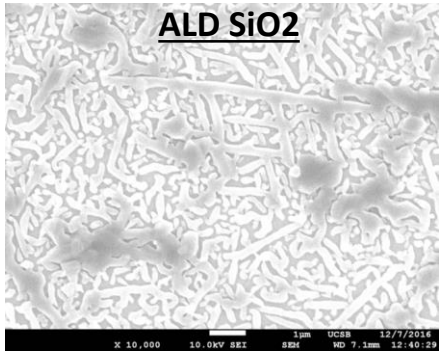


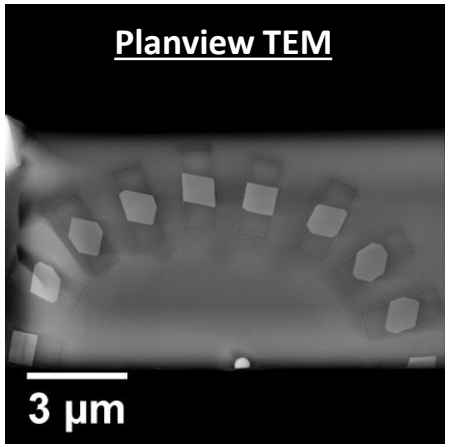


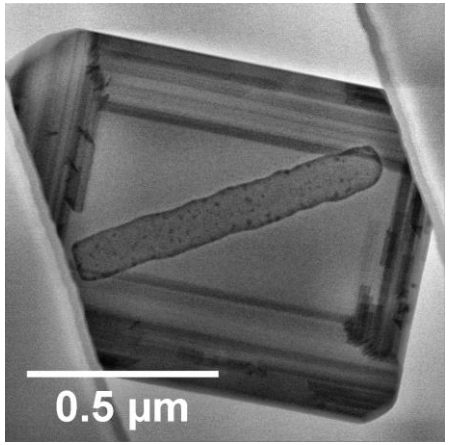
Design Considerations (III-V)

1. Growth Selectivity
   - Not all oxides are created equal, chose wisely
2. Growth Window Definition
   - Exposing surfaces to ion damage is bad for growth
   - May need very small opening → dry etch → etch stop, careful while stripping
3. Sacrificial Layer
   - Defines cavity geometry/edges
   - Must be easily/selectively removed (resist or Si)
4. **Characterization**
   - How to determine what is good and bad
   - Simple electrical tests are not as simple due to parasitic growth



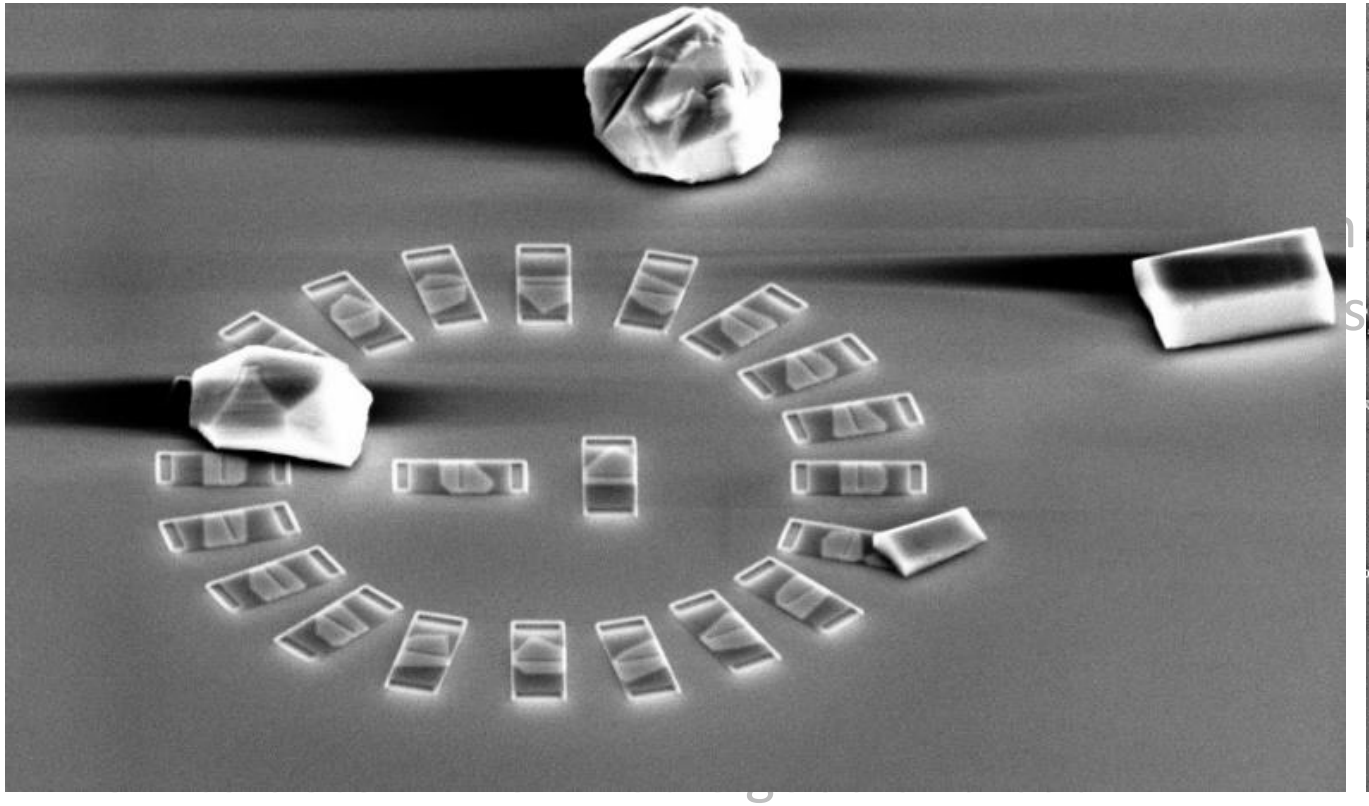


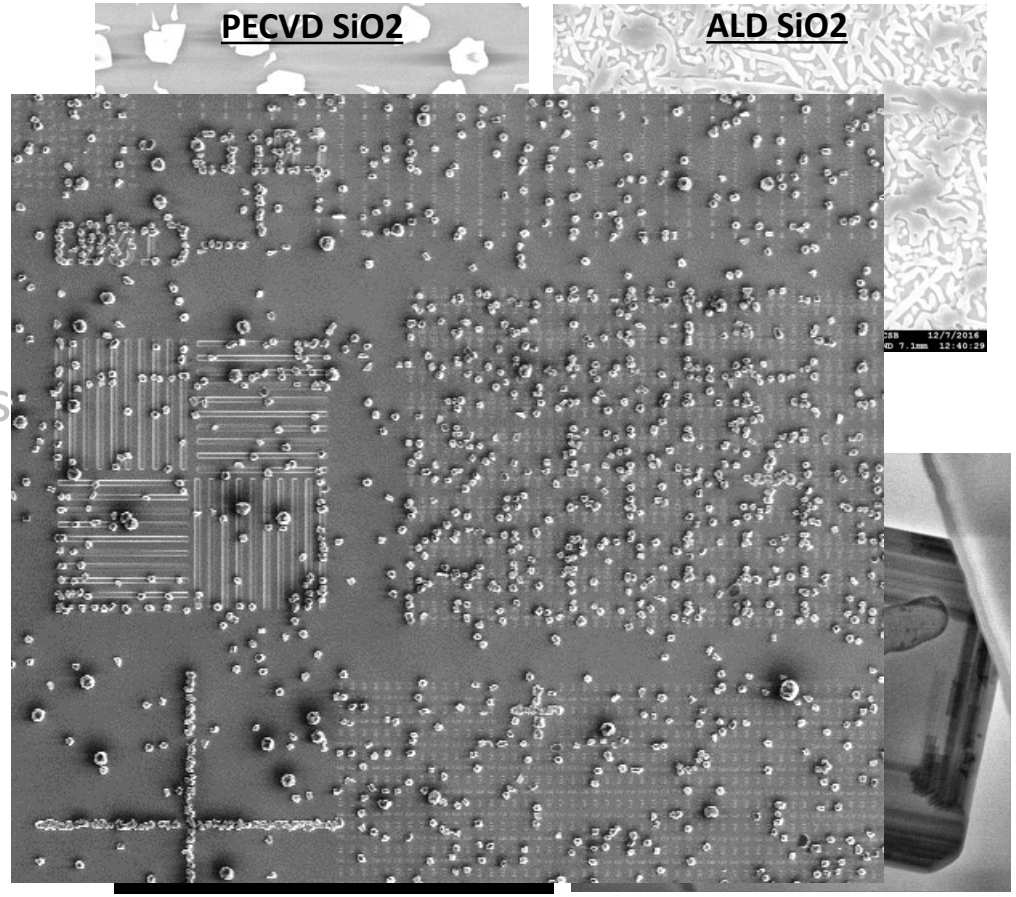




Design Considerations (III-V)

1. Growth Selectivity





2.

3.

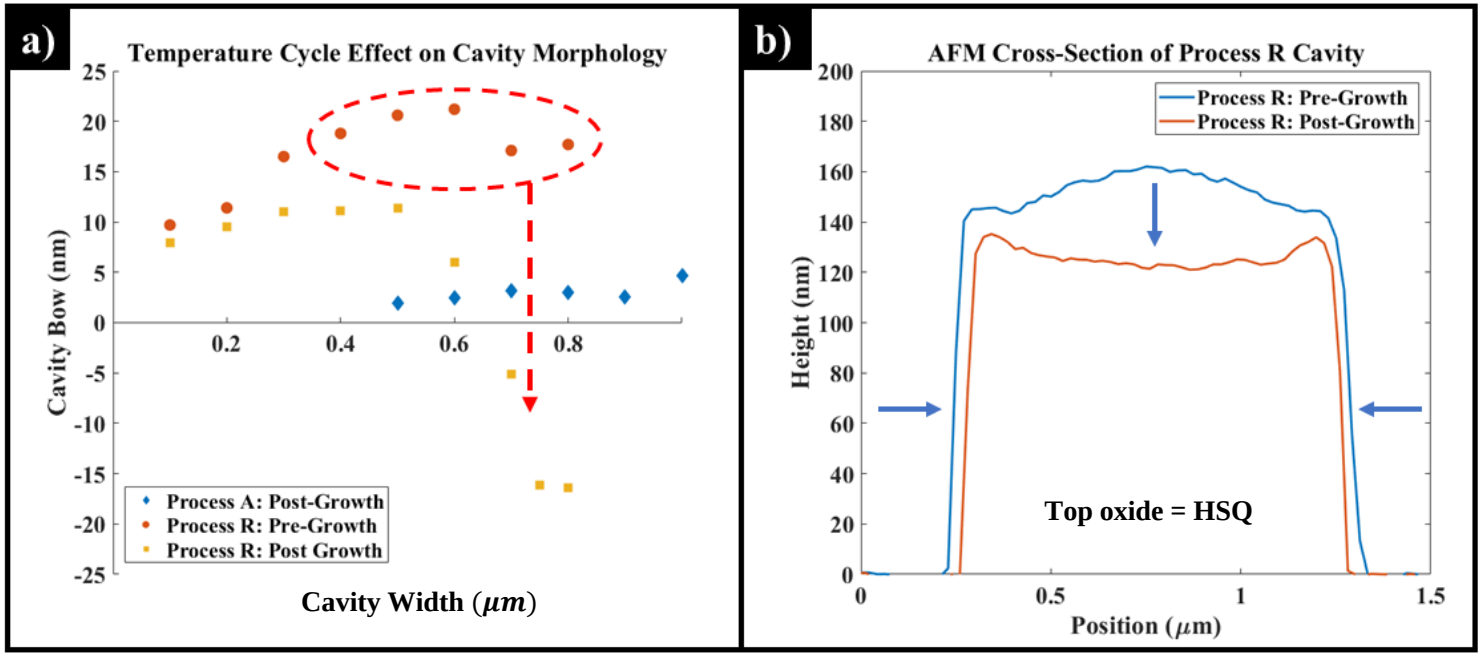
4.

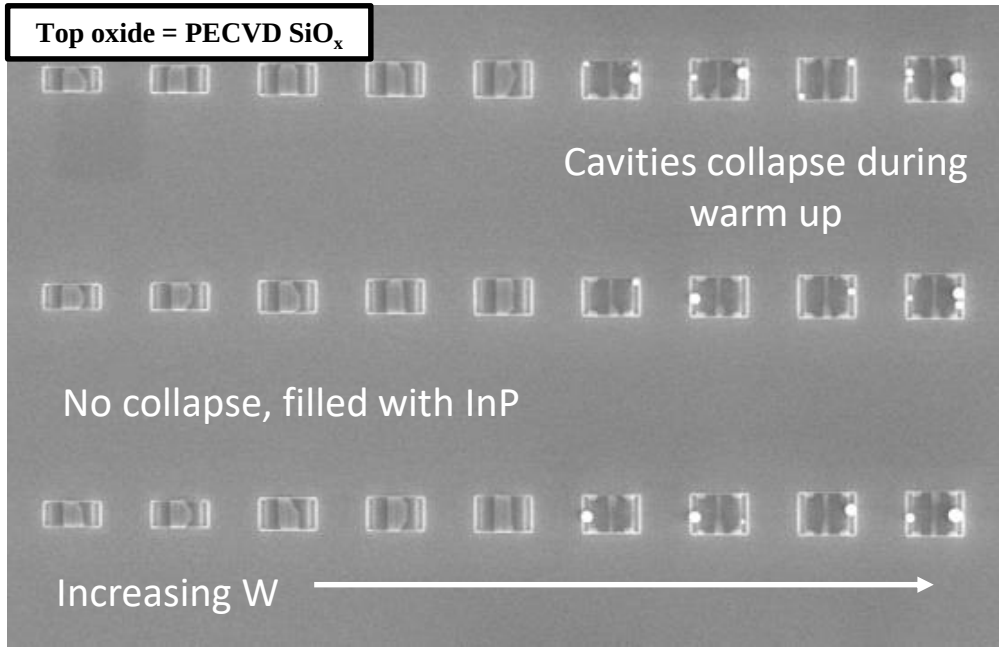
- Simple electrical tests are not as simple due to parasitic growth

5. **Top oxide → defines selectivity & cavity when empty → can we process?**

Design Considerations (III-V)

Top Oxide: What happens to your cavity during growth (600°C)?





Temperature cycles, oxide chemistry, and mechanical rigidity all come into play

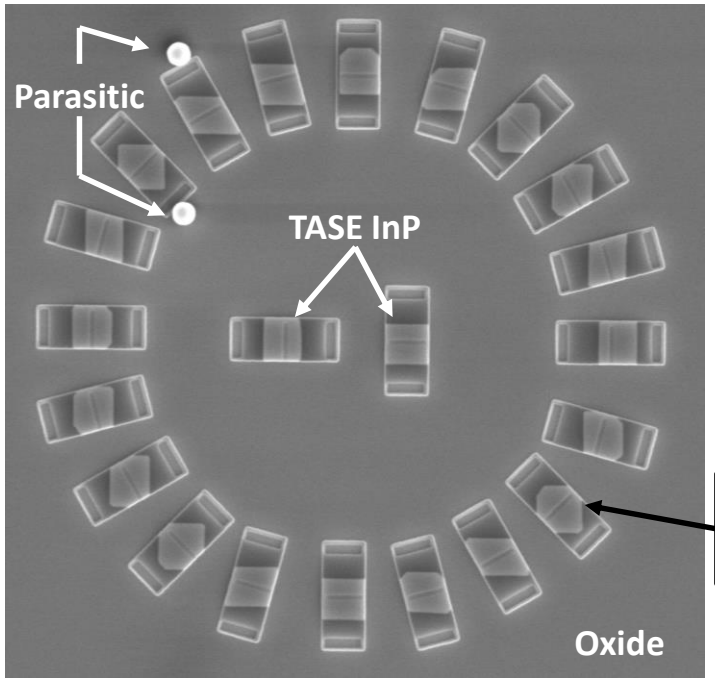
Must pay very close attention to your (top) oxide → before, during, and after

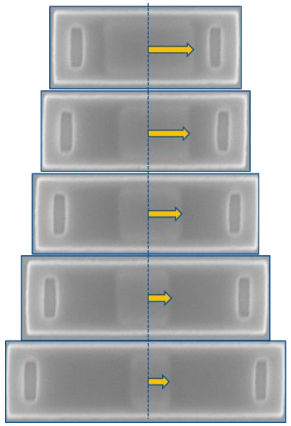
1. **MOS-HEMT Introduction**
   - Beyond 5G Application
   - Design Challenges
   - Proposed InAs/InP MOS-HEMT Design
2. **THz Transistor "Pieces"**
   - Fabrication Process
   - High-k Quality
   - Modulation Doped Access Regions
   - $f_\tau = 480\ GHz$ MOS-HEMT demonstration
3. **Template Assisted Selective Epitaxy (TASE) Introduction**
   - Heterogenous Integration & Heterojunction Turning
   - Design Challenges & Fabrication Process
4. **TASE Examples**
   - Homo-epitaxy
   - Hetero-epitaxy
5. **Conclusions**

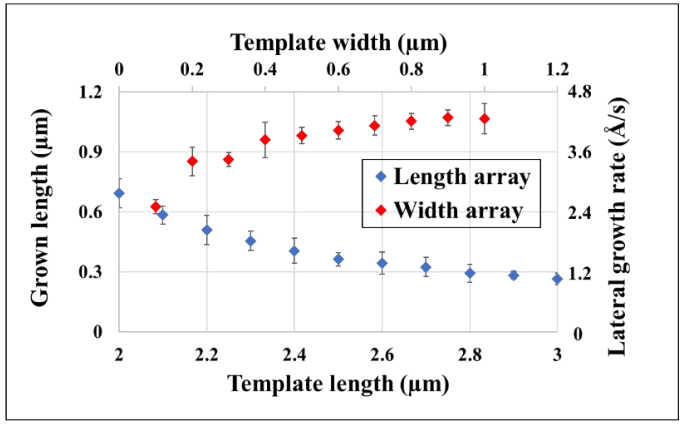
Homo-epitaxy: InP / InP

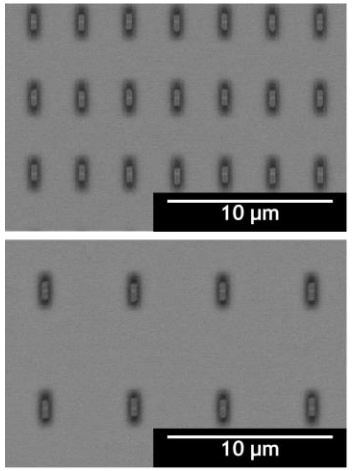
- Easiest place to start → how do things grow inside boxes?

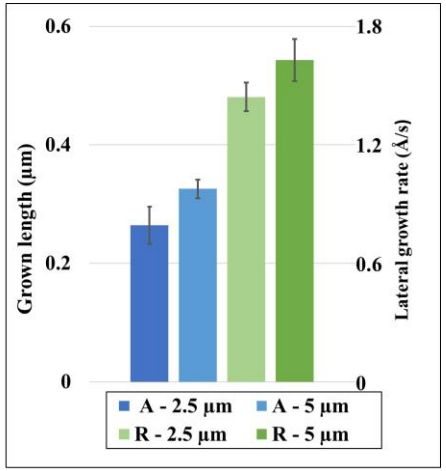
Homo-epitaxy: InP / InP – Growth Dynamics







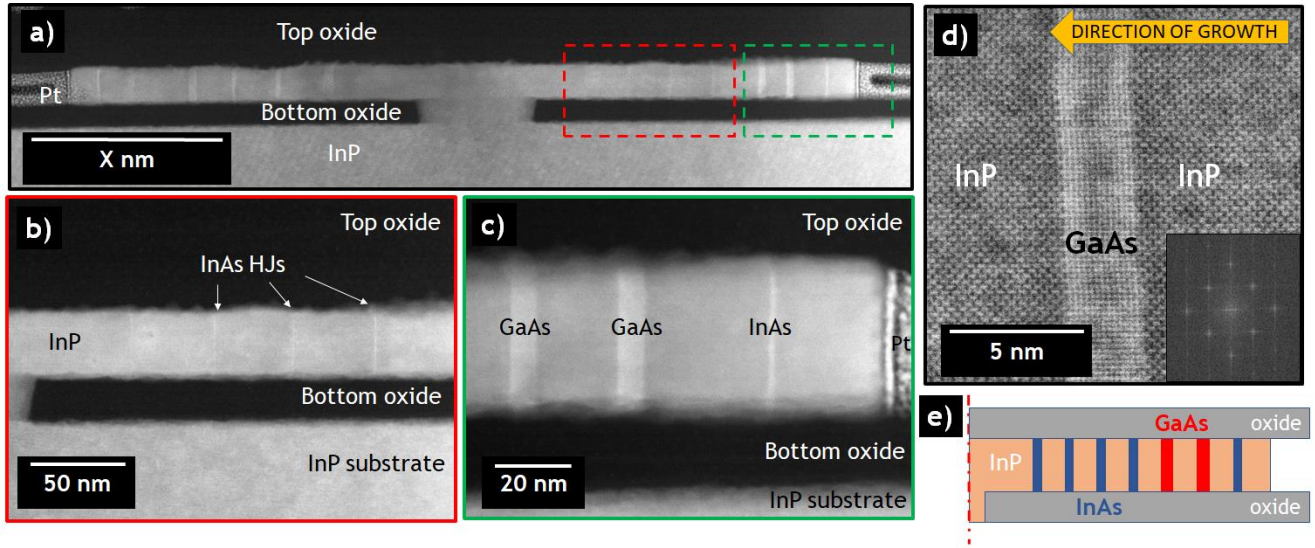




Facets determined by growth conditions, not cavity

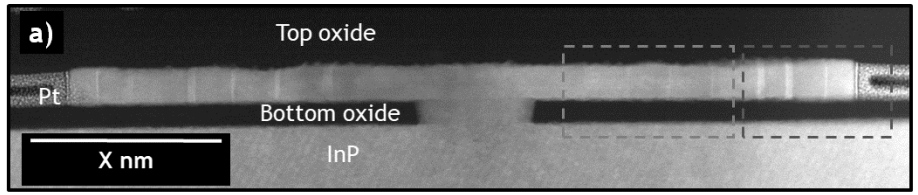
- Facets controlled by growth conditions (Temperature & V/III ratio → use low P)
- Increasing cavity thickness and width increases growth rate
- Decreasing cavity length and pitch (packing density) increases growth rate
- Control/uniformity/reproducibility are always challenging

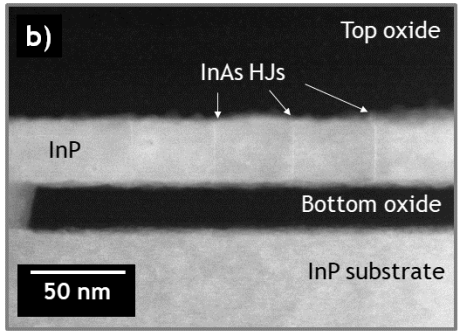
Homo-epitaxy: InP / InP – Quantum Wells

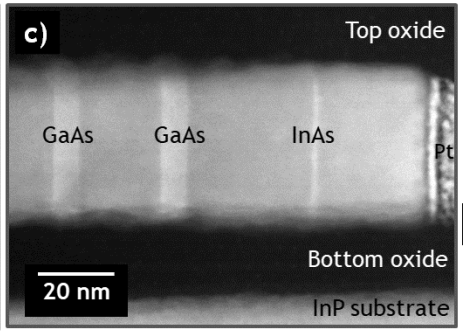


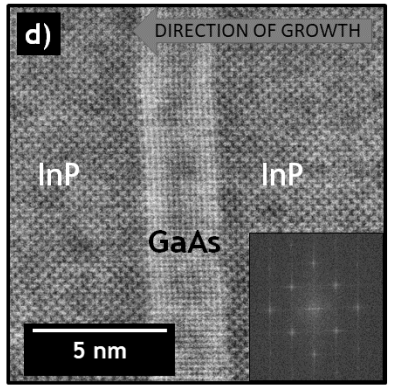
- Pseudomorphic GaAs and InAs quantum wells
- Atomically abrupt interfaces
- Often issues with missing HJs, inconsistent well width

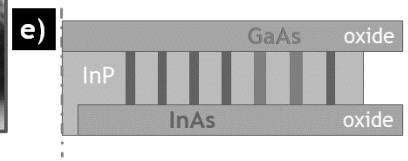
Homo-epitaxy: InP / InP – Quantum Wells

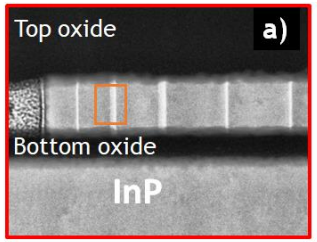


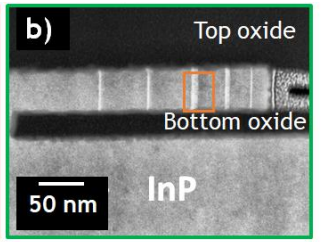


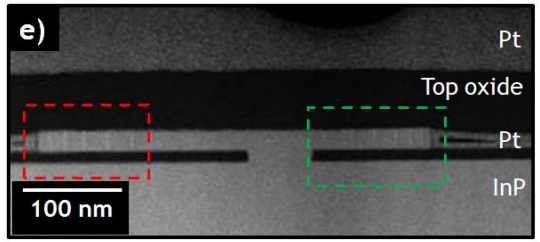


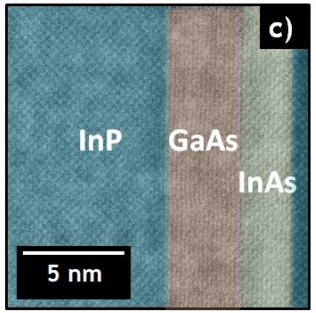


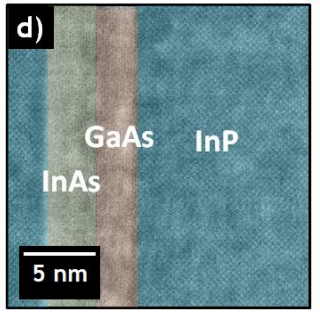


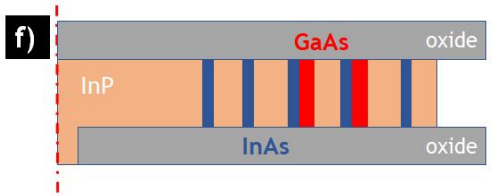












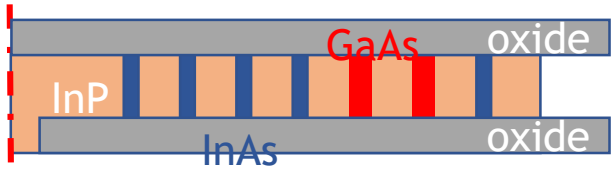
- Pseudomorphic GaAs and InAs quantum wells
- Atomically abrupt interfaces
- Often issues with missing HJs, inconsistent well width

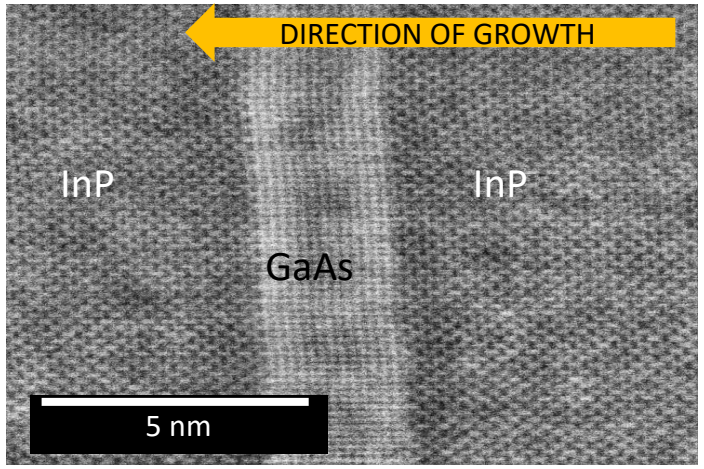
- Example of 3HJ-TFET design
- Strain compensated 3HJ (GaAs = tensile, InAs compressive)

Homo-epitaxy: InP / InP – Quantum Wells

Strained Single Quantum Wells

Material: InAs and GaAs
Device: LED or LASER
Application: Displays, commun.





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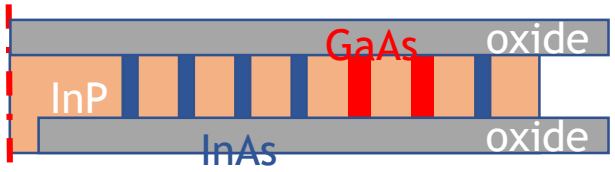
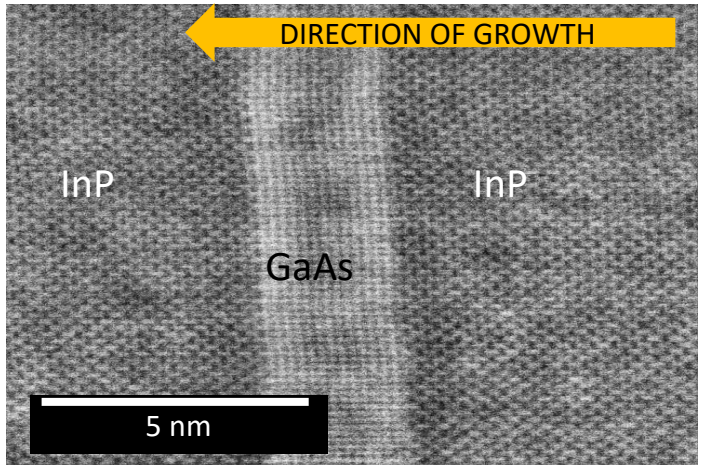
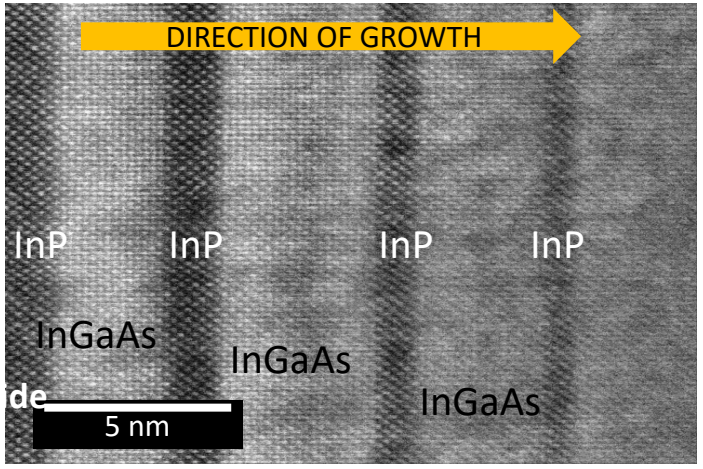




Super Lattice

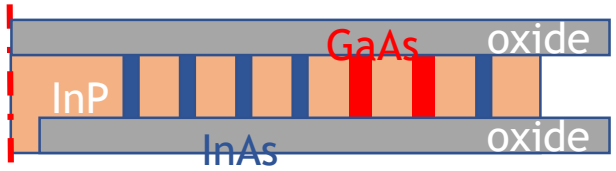
Material: InGaAs/InP superlattice
Device: Superlattice FET
Application: Low Power Logic

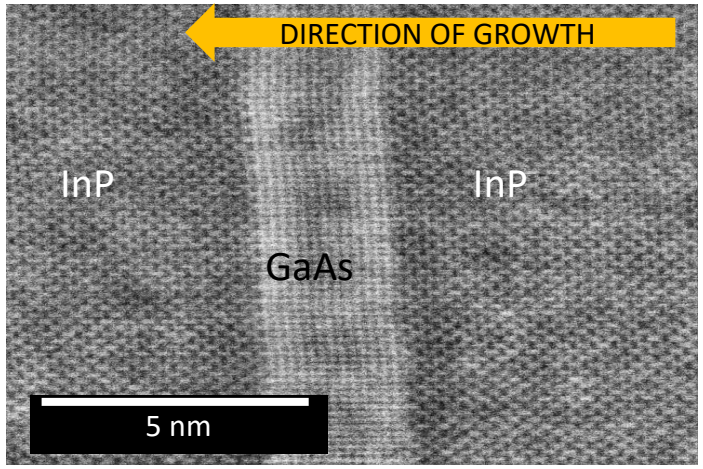


Homo-epitaxy: InP / InP – Quantum Wells

Strained Single Quantum Wells

Material: InAs and GaAs
Device: LED or LASER
Application: Displays, commun.





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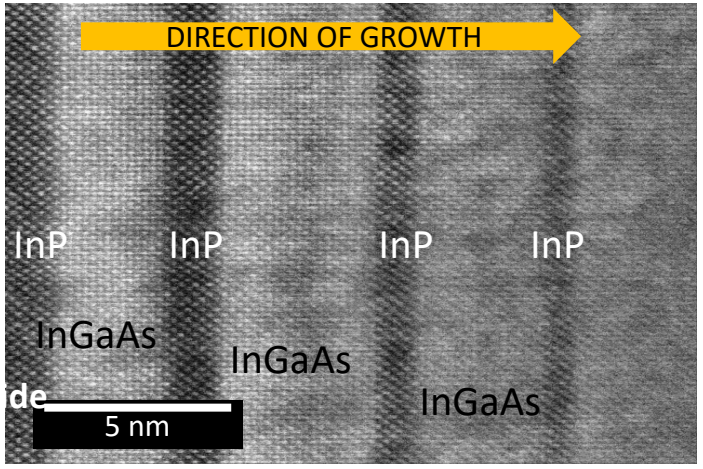
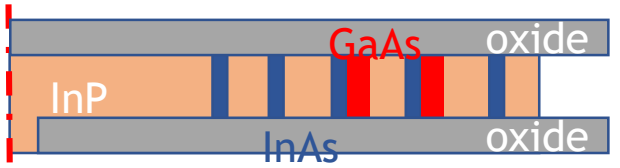
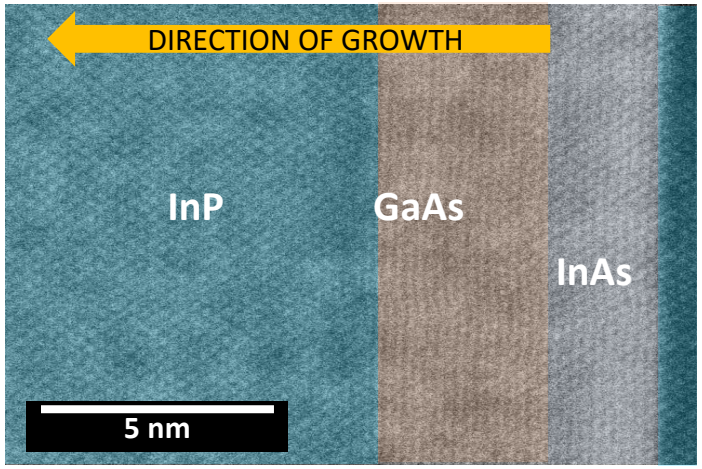


Triple Heterojunction

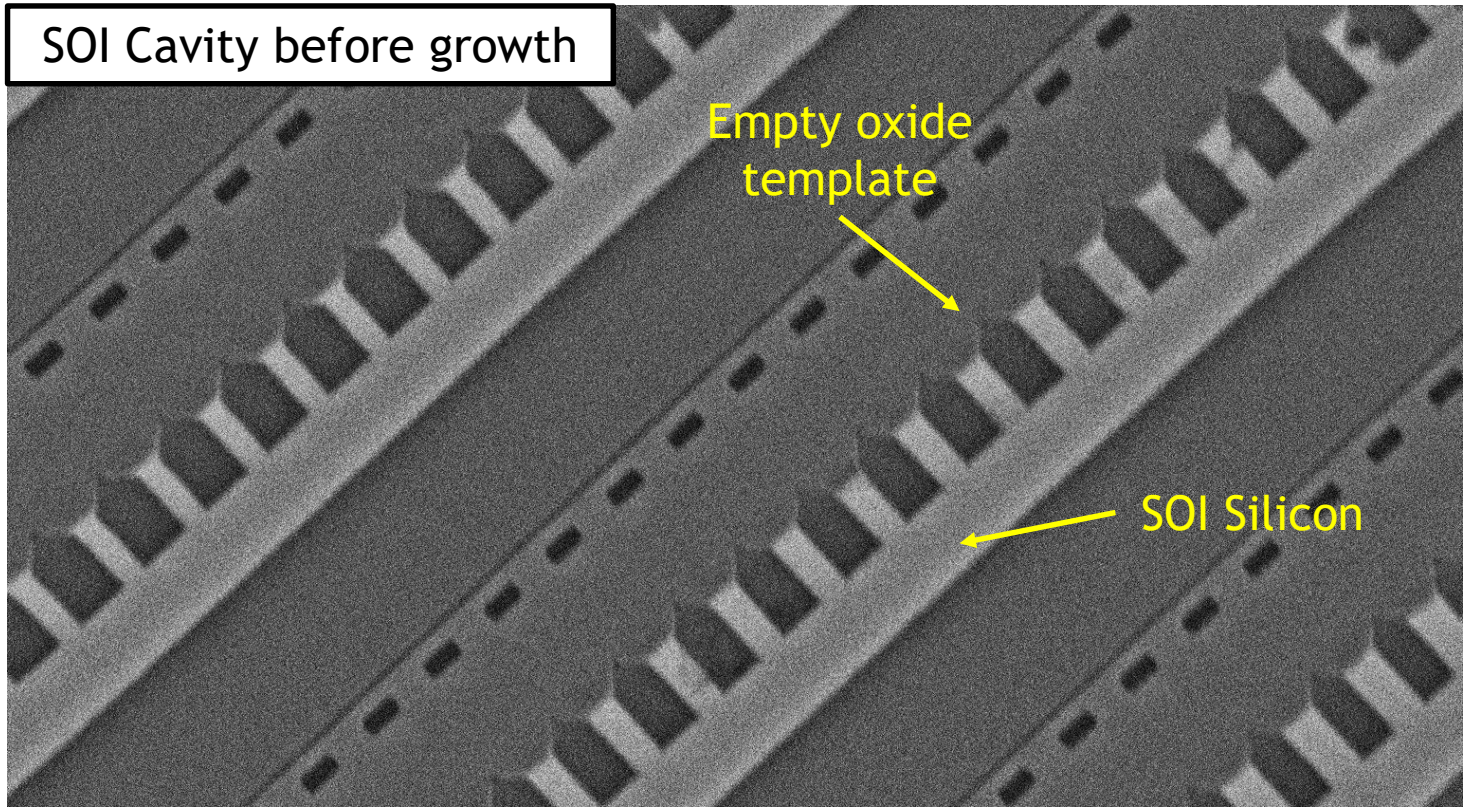
Material: InP/InAs/GaAs/InP
Device: 3HJ TFET
Application: Low Power Logic



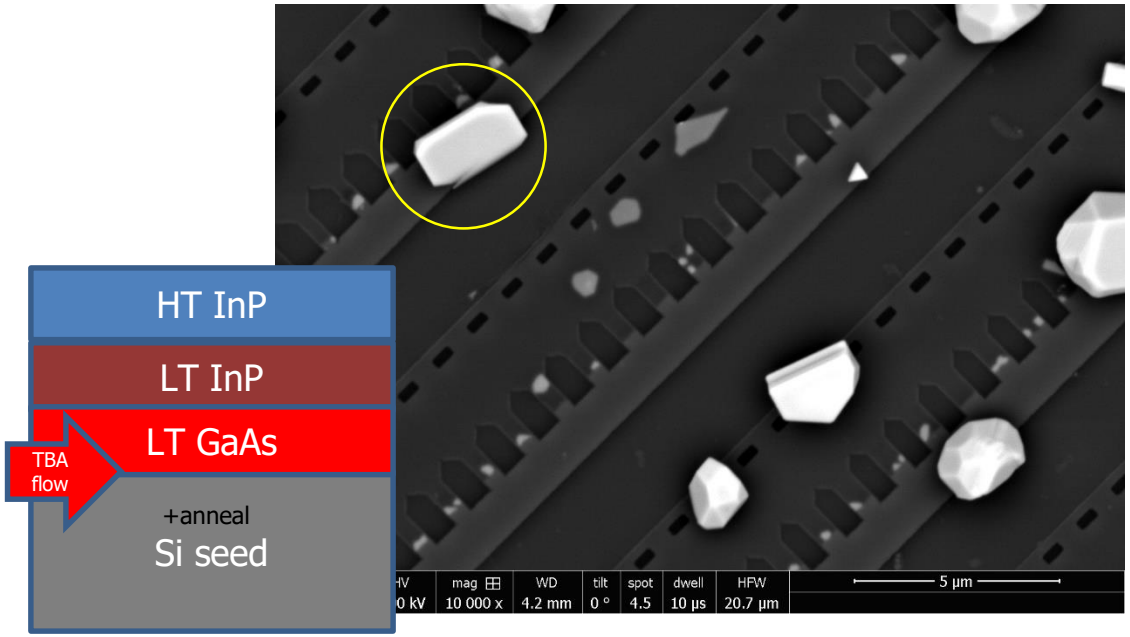


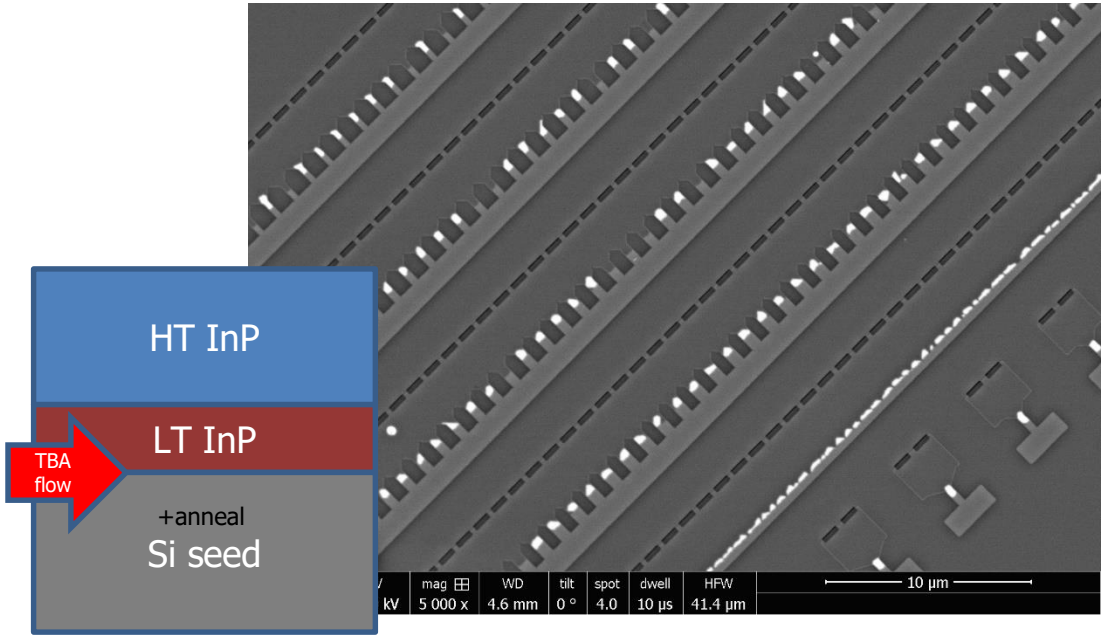
Hetero-epitaxy: InP / SOI

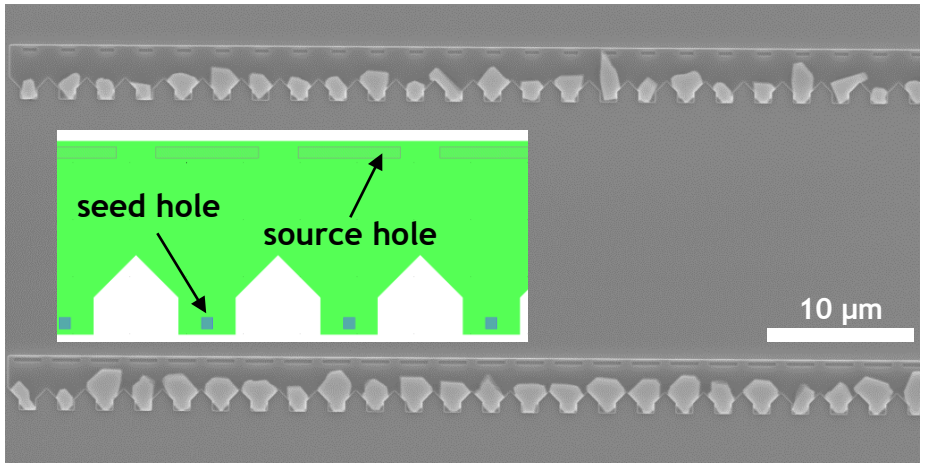
- Nucleation is harder → severe lattice mismatch
- Tricks that work for selective area growth with large fill factor (low temperature nucleation) unlikely to work for TASE

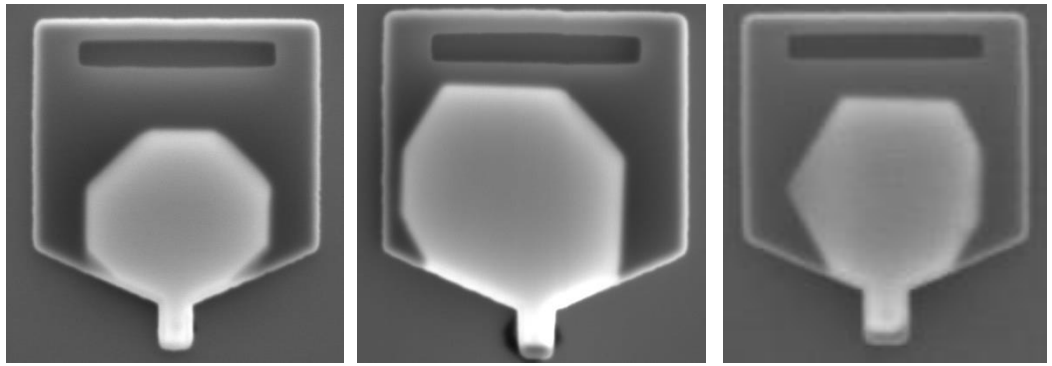


Hetero-epitaxy: InP / SOI & Si

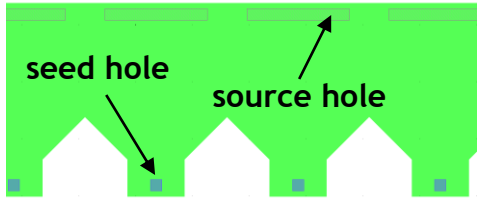




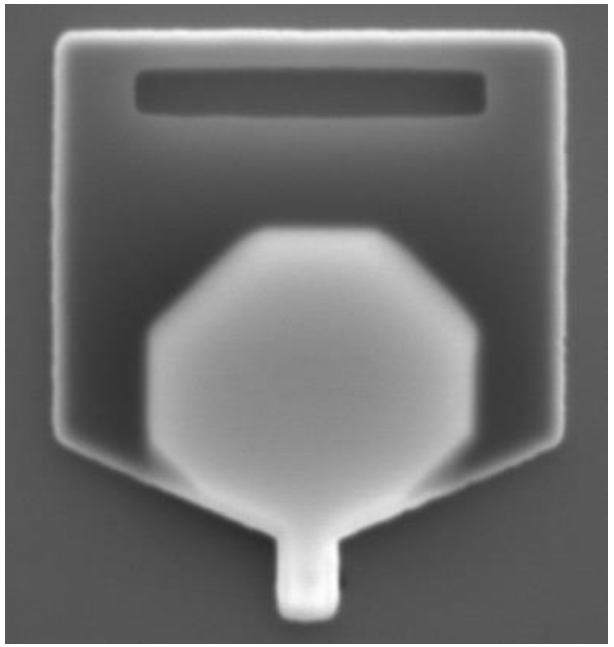


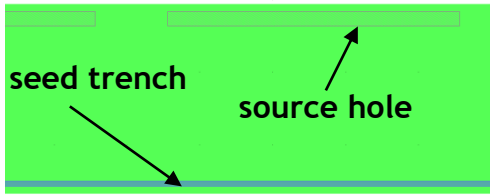


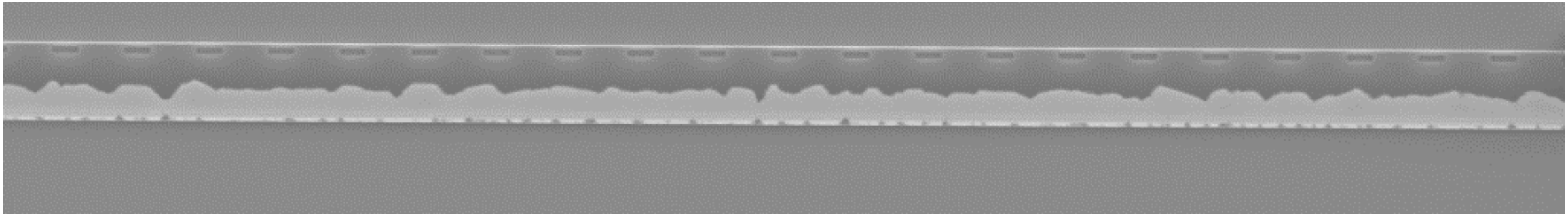
Hetero-epitaxy: InP / Si



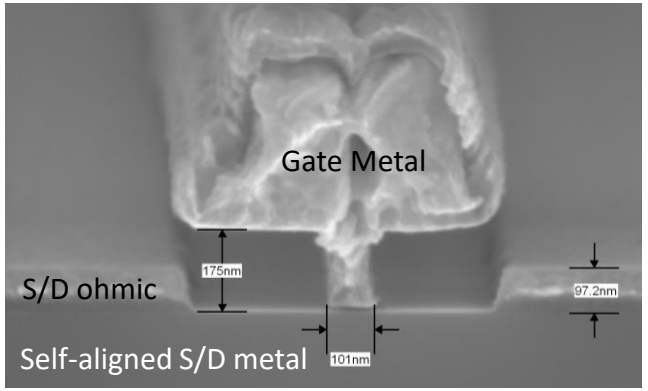
- Single point nucleation appears easier
- Currently working to scale up to ASML
  - Higher packing density
  - Higher throughput
  - Lower cost
  - If needed, 1st litho step (seed) can be done by EBL





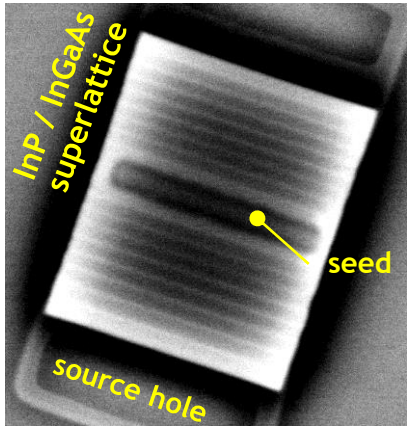


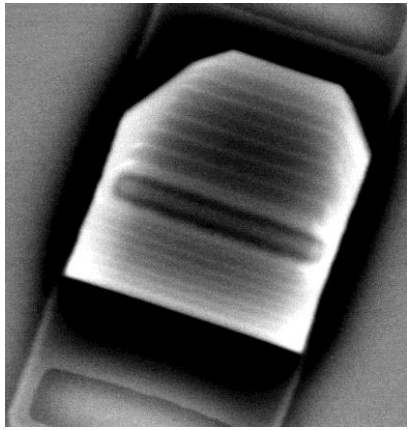
Conclusions



MOS-HEMT:

1. Demonstration of process, minor tweaks for big wins
2. Bottom up process gives some process freedom compared to top down
3. T-Gates (alignment & filling) are **TOUGH…**





TASE:

1. Opens a new degree of freedom in device design
2. Heterogenous integration on Si (electronics) and SOI (photonics)
3. Processing (very sensitive) + Growth (very sensitive) = **VERY SENSITIVE**

Acknowledgements

Professors: Prof. Mark Rodwell, Prof. Jonathan Klamkin, Prof. Chris Palmstrom

Funding Support: SRC, DARPA, NSF (ComSenTer, JUMP, E2CDA)

Rodwell Team: (Past and Present)

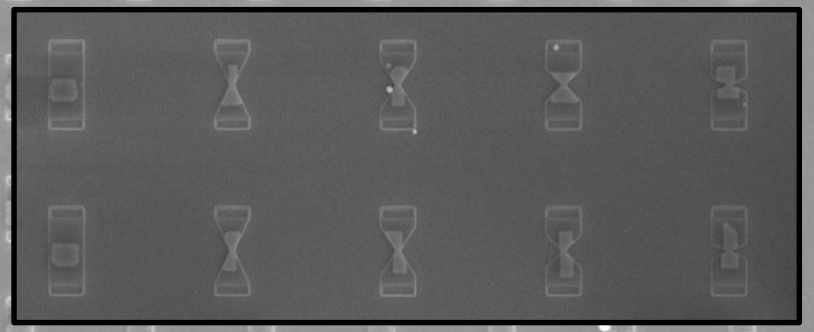
- **Device:** Hsin-Ying Tseng, Yihao Fang, and Jun Wu
- **Circuits:** Arda Şimşek, Ahmed Samir, Ali Farid, Utku Soylu, Rob Mauer
- **Past/Administrative:** Cheng-Ying Huang, Sanghoon Lee, Andy Carter, Prateek Choudhary, Johann Rode, Miguel Urteaga, Audra Pierce

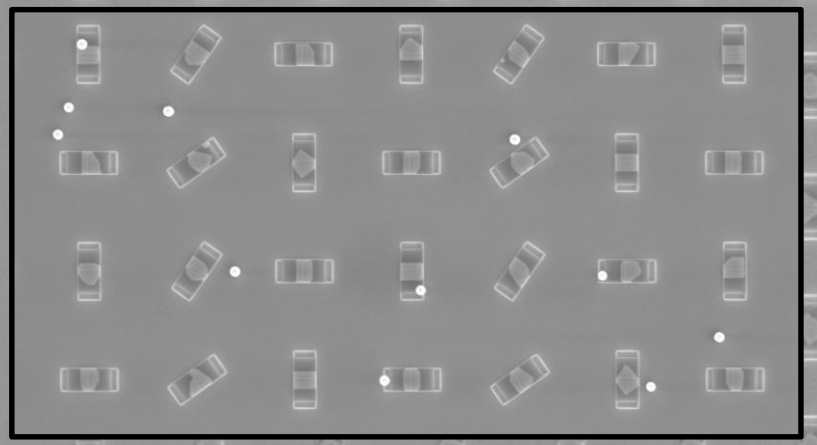
MOCVD Growth: Simoné Tommaso Šuran Brunelli, Bei Shi, Klamkin Group, Palmstrom Group

Characterization: Aranya Goswami, Palmstrom Group

Special Thanks: Cleanroom Staff and MOCVD Staff

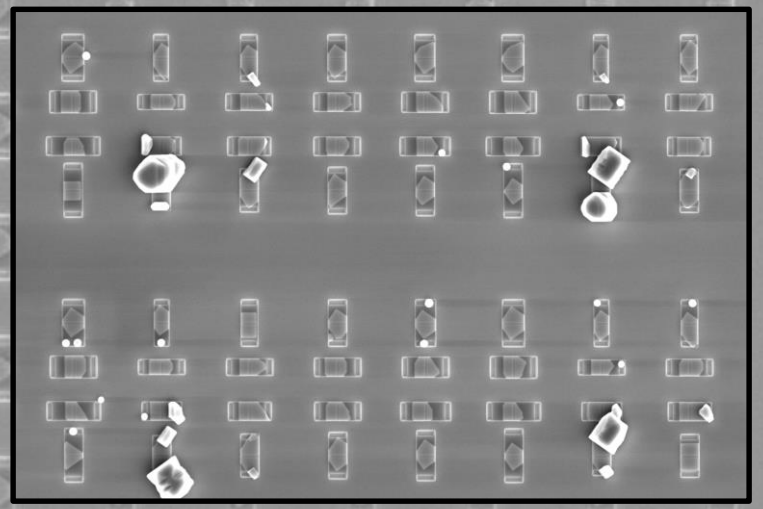
UCSB Community → that's all of you ☺

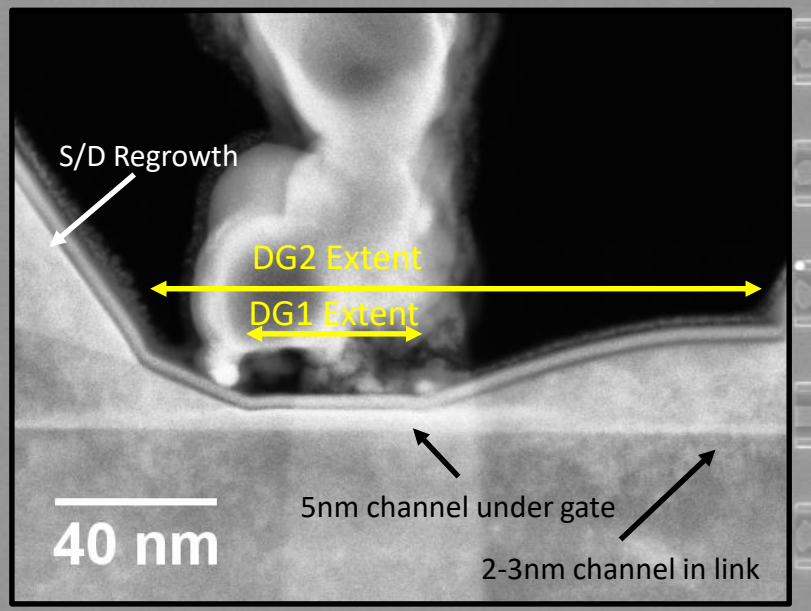




Thank You

Questions?





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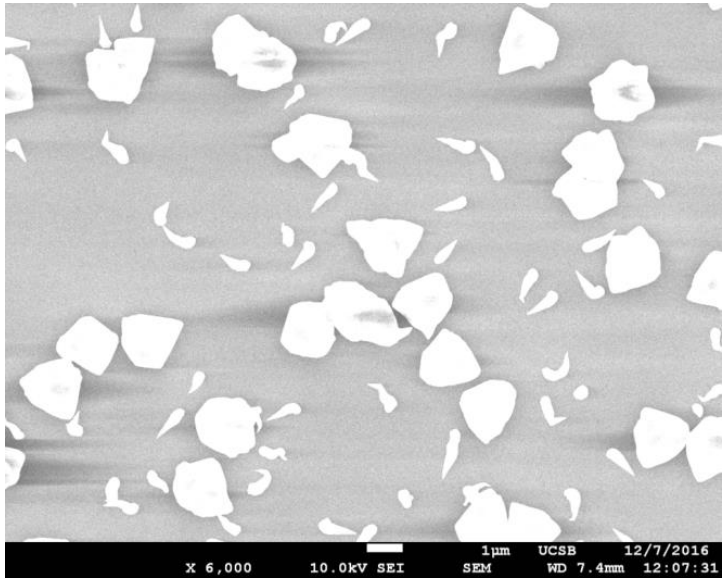
9. V. Chobpattana "Highly Scaled High Dielectric Constant Oxides on III-V CMOS with Low Interface Trap and Low Leakage Densities," *Doctoral Dissertation*, University of California Santa Barbara, Santa Barbara, 2016.

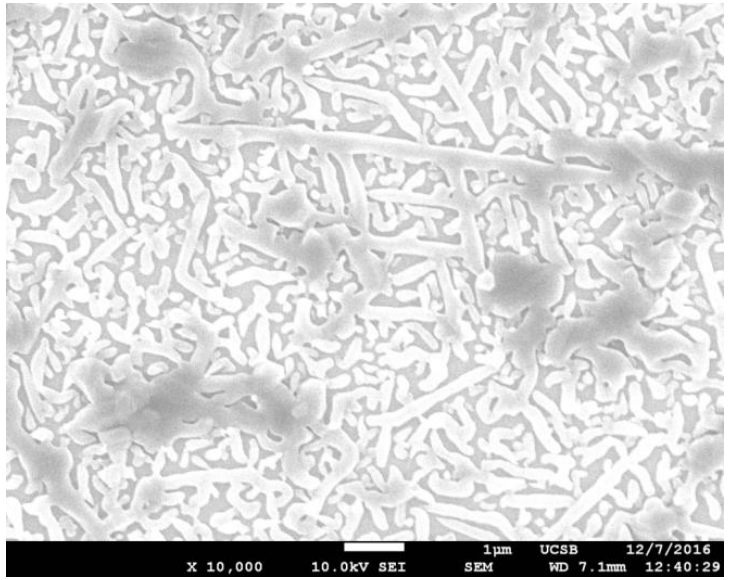
Design Considerations

1. Growth Selectivity → **Inherently low fill factor, don't want material nucleating where its not supposed to**

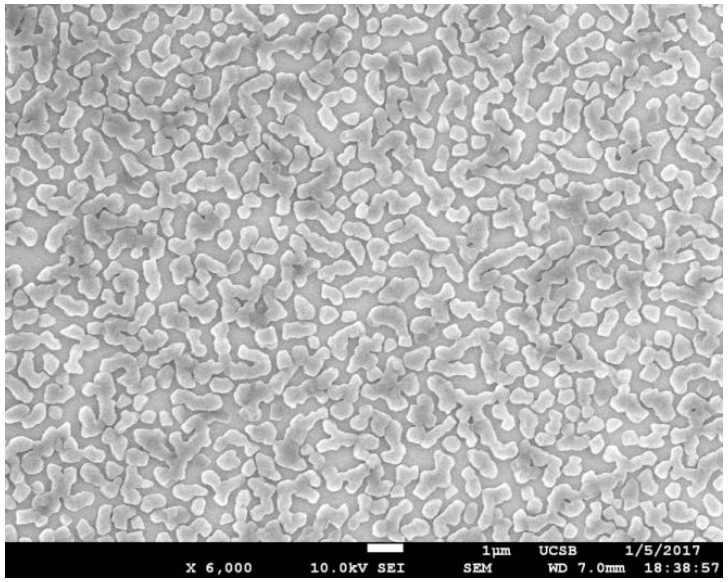
PECVD SiO2



ALD SiO2

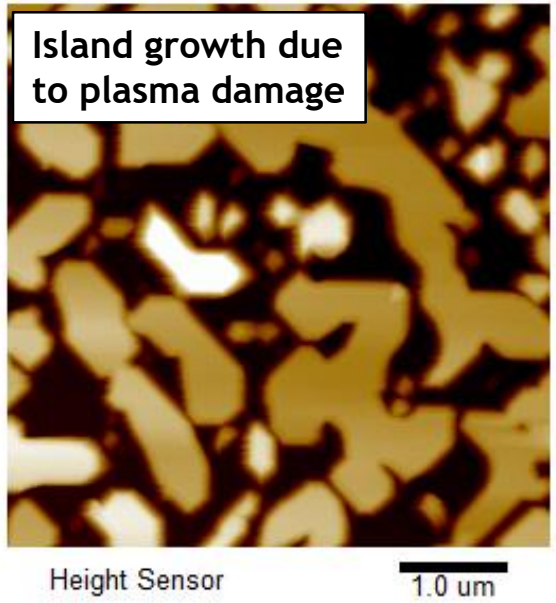


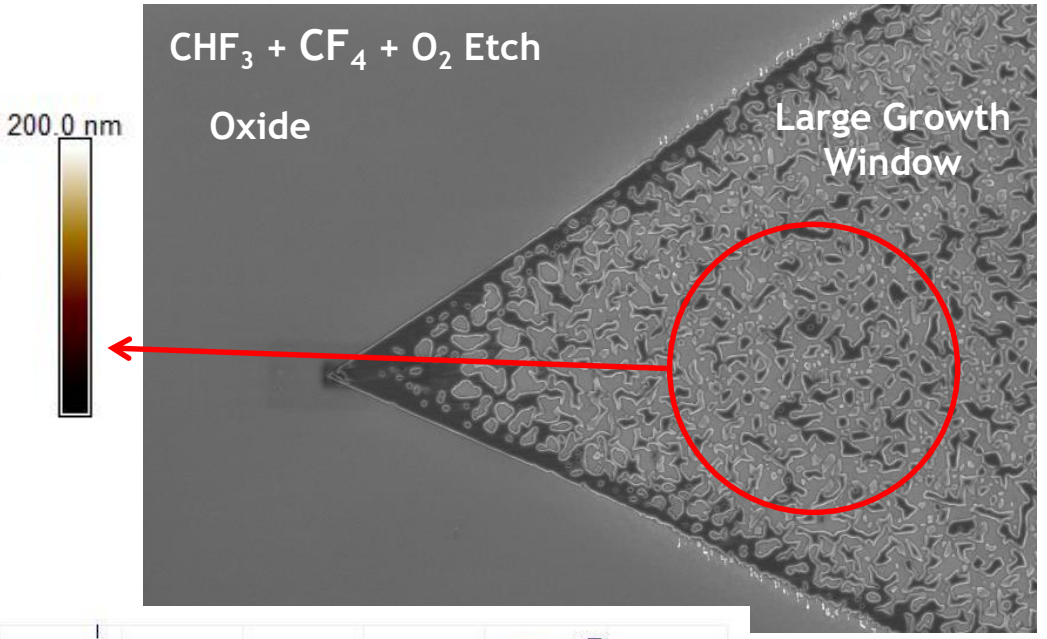
Sputtered SiO2

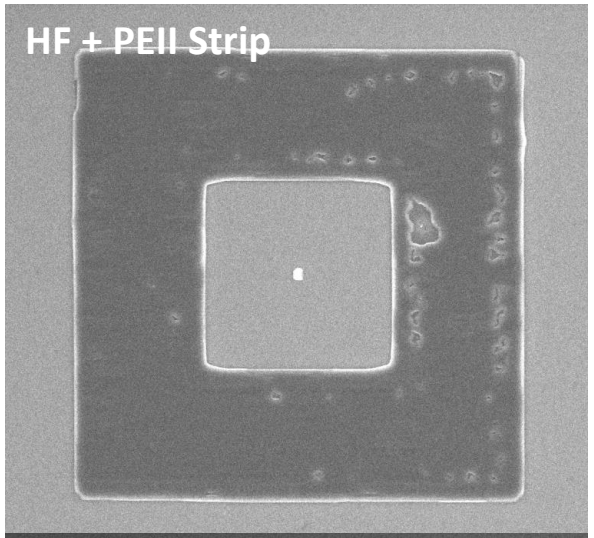


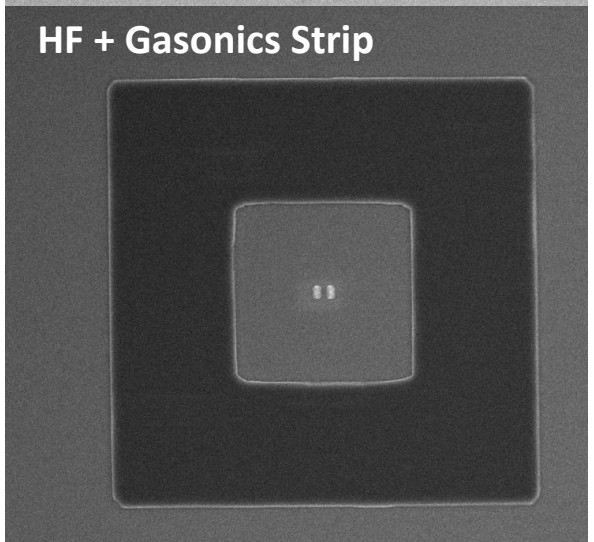
Design Considerations

2. Growth Window Definition → **Don't want to damage interface before growth, can cause poor initiation**



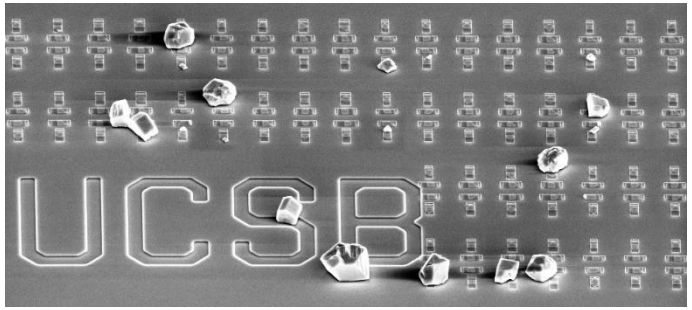


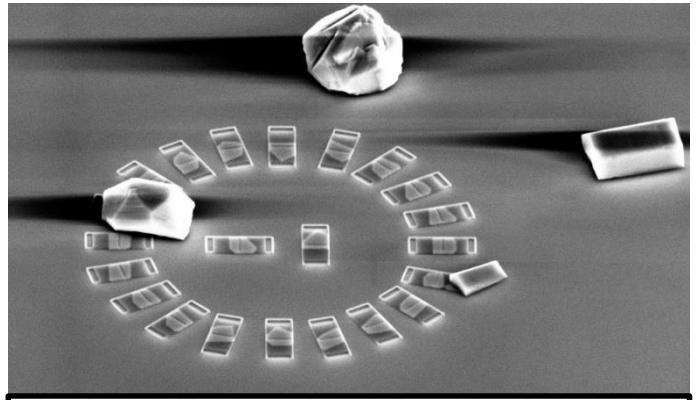




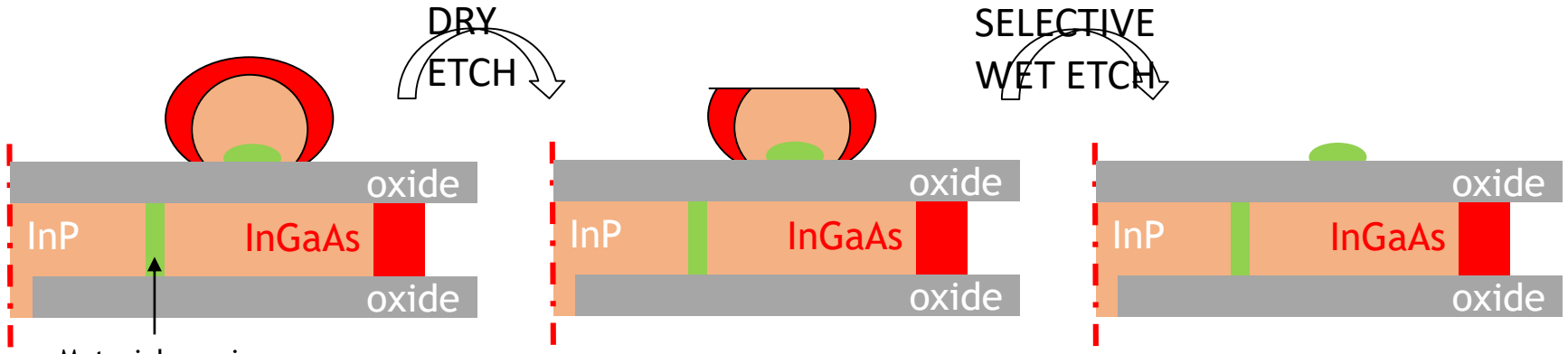
Design Considerations

3. Post-processing → **Need to be able to make devices!**
   - **Parasitic growth makes lift-off difficult → ruins resist profile**
   - **Growth on alignment mark edges makes alignment difficult**





Parasitic size ~2-4 μm diameter



Parasitics on alignment marks